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Self-aligned Graphene Field Effect Transistors With Surface Transfer Doped Source/Drain Access Regions

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Self-aligned Graphene Field Effect Transistors With Surface Transfer Doped Source/Drain Access Regions

by

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Thesis

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Abstract

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by

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The University of Texas at Austin, 2012

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Since its discovery in 2004, graphene has been widely touted as a potential replacement for silicon in the next generation of electronic circuits owing to its exceptionally high carrier mobilities and its ultra-thin body. Graphene field effect transistors (GFETs) show promising potential for use in analog and radio frequency (RF) applications, with theoretically predicted THz frequencies only being limited by fabrication challenges. High series resistance of the source/drain access regions in a GFET is one such major factor responsible for performance degradation. In this thesis, a simple and straightforward scheme of reducing this resistance by self-aligned spin-on-doping of graphene using surface transfer dopants is presented.

Back-gated GFETs were fabricated on Si/SiO_2 and doped using various surface transfer dopants. A novel method of spin-on-doping graphene using poly(ethylene imine) (PEI) was developed. Top-gated GFETs with mobilities up to 6,900 cm^2/Vs were fabricated and their access regions were spin-on-doped in a self-aligned manner offering a 3X reduction in the series resistance. GFET drive currents improved by up to 4X and transconductances up to 3X after self-aligned doping. GFETs were also fabricated on insulating quartz substrates with mobilities up to 5,600 cm^2/Vs and showed performance enhancements up to 2X after self-aligned doping.

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Introduction

1.1 Current state of CMOS

Moore's Law [1] has been the major driving factor behind silicon complementary metal oxide semiconductor (CMOS) scaling for more than four decades. Scaling down the critical dimensions of a metal-oxide-semiconductor field-effect transistor (MOSFET) has multiple advantages - smaller, faster and cheaper transistors. However, there are fundamental limits on how small a transistor can be made before quantum mechanical effects start compromising basic transistor functionality.

One of the critical device parameters that takes a major hit due to continued scaling is the gate-leakage current. As the gate dielectric (SiO_2) thickness falls below 1.3 nm, direct electron tunneling results in intolerably large leakage currents [2]. This leakage current over many millions of transistors on a chip results in a large power dissipation which could burn out the chip. In the current generation of CMOS transistors, this problem has been mitigated by using high-κ dielectric materials like HfO_2 in place of SiO_2 [3].

The International Technology Roadmap for Semiconductors (ITRS) has identified

a need for new materials and structures with significantly improved properties to meet future technology requirements [4]. An evolutionary approach is to look at newer device architectures like extremely-thin (ET) SOI, multiple gate FET (MuGFET) and gate-all-around FET (GAA FET) or to replace silicon with materials like strained Si, SiGe and III-V compound semiconductors (Figure 1.1).

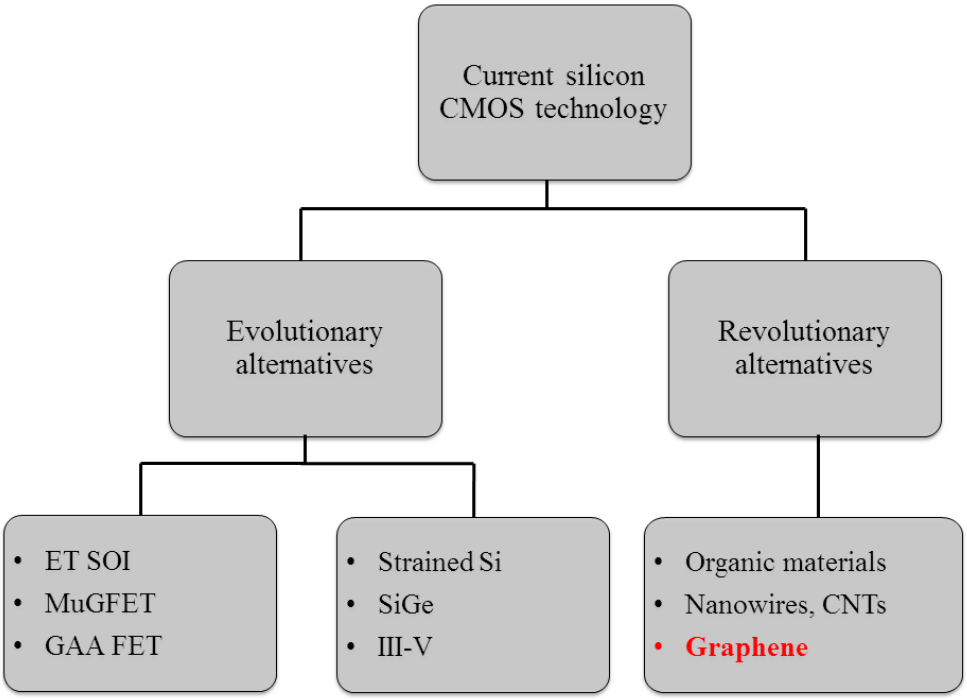


Figure 1.1: Replacement options for current silicon CMOS technology

A more radical and revolutionary approach is to look beyond silicon-based electronics. Recent advances in nanotechnology have opened up new avenues in the form of novel materials like nanowires, carbon nanotubes (CNTs) and organic materials with exotic electronic properties that can be used as replacements for silicon (Figure 1.1). Graphene is one such material with interesting properties that has the potential to replace silicon for post-CMOS applications.

1.2 Graphene for post-CMOS

Graphene is a two dimensional, single atom thick layer of carbon atoms arranged in a hexagonal honeycomb lattice. Graphene was thought to be a fictional material that could not exist in reality until its experimental discovery in 2004 [5]. It is considered the basic building block for all other graphitic materials - it can be wrapped up into 0D fullerenes, rolled into 1D nanotubes or stacked into 3D graphite as shown in Figure 1.2 [6].

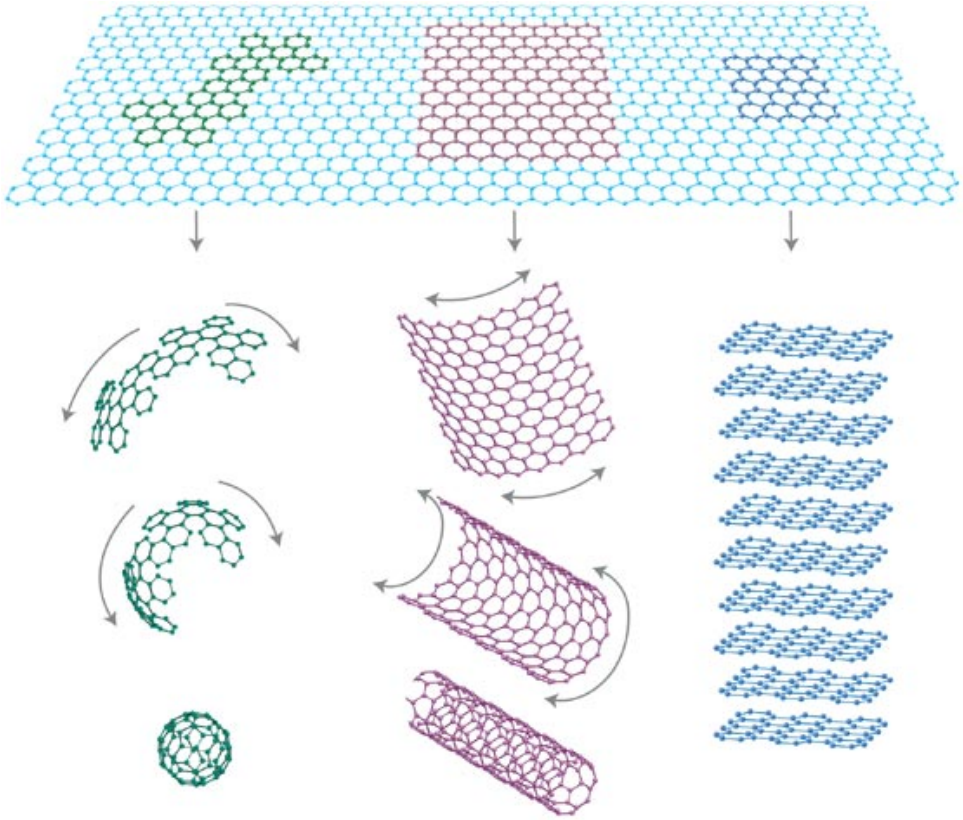


Figure 1.2: Fullerenes, nanotubes and graphite are derivatives of graphene [6]

Carbon atoms in graphene are sp^2-bonded with each other. The strong σ-bonds between adjacent carbon atoms are responsible for its exceptional mechanical stability. The p_z orbitals, which are perpendicular to the graphene plane are involved in weak π-

bonding. The electrons involved in these π-bonds are delocalized and are responsible for the interesting electronic properties of graphene [7].

Graphene is considered to exhibit one of the highest carrier mobilities of all known materials. Researchers have found that charge carriers in graphene have mobilities of the order of 10,000 cm^2/Vs even at room temperature [6], whereas carrier mobilities in Si are only of the order of 1,000 cm^2/Vs. These high carrier mobilities make graphene a promising material for ultra-fast electronics operating at THz frequencies [6].

Owing to the large mobility and high current carrying capability (about 1×10^8 A/cm^2) of graphene, it may also be useful for radio frequency (RF) applications [8]. Electrons also have a long spin relaxation time in graphene which makes it possible to engineer graphene-based spintronics devices, where the spin of the electron is used as a state variable for logic [9].

The conduction and valence bands of monolayer graphene touch at the Dirac point, making it a zero bandgap semiconductor. Bilayer graphene on the other hand can be tuned electrostatically to open up a bandgap [10]. Novel devices like the bilayer pseudo-spin field effect transistor (BiSFET) which use the unique intrinsic properties of graphene have also been proposed and are being currently researched [11].

Graphene nanoribbons (GNRs) are another avenue of research. GNRs are graphene nanostructures with confinement in one dimension. GNRs can be engineered depending on their crystallographic orientation to be metallic or semiconducting [12].

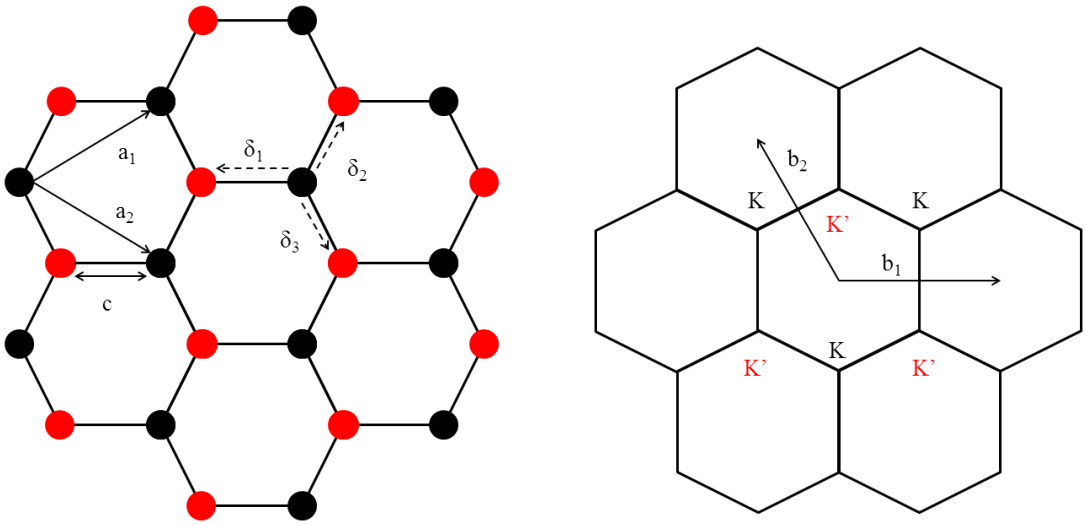
Graphene processing is compatible with traditional CMOS technologies. Its planar geometry makes it the ultimate ultra-thin body channel material and it is less likely to suffer from performance degradation due to scaling. Graphene can be an evolutionary replacement to conventional CMOS where it replaces Si as the channel material, or a revolutionary replacement where alternative switching mechanisms can be developed using the unique properties of graphene [13].

1.3 Graphene: Properties

Most of the exotic electronic properties of graphene are a direct consequence of its bandstructure. Electrons in graphene behave like relativistic, mass-less particles around the Dirac point and this gives rise to many quantum electrodynamics (QED) effects.

Bandstructure of graphene

Figure 1.3(a) shows the real space lattice of graphene. The lattice is hexagonal with lattice vectors $\mathbf{a}_1$ and $\mathbf{a}_2$ and has a two-atom basis (shown as black and red circles). The C-C bond length (c) is 1.42 $\mathring{A}$. Figure 1.3(b) shows the reciprocal lattice.



(a) Real space lattice of graphene (b) Reciprocal lattice of graphene

Figure 1.3: Real space and reciprocal lattices of graphene

The tight-binding Hamiltonian for the graphene lattice is given by Equation 1.1 and Equation 1.2 [13]. The Hamiltonian can be diagonalized to obtain the spectrum $E(\mathbf{k}) = \pm|f(\mathbf{k})|$.

$$h(\mathbf{k}) = -\begin{pmatrix} 0 & f(\mathbf{k}) \\ f^*(\mathbf{k}) & 0 \end{pmatrix} \tag{1.1}$$

$$f(\mathbf{k}) = t(e^{i\mathbf{k}.\delta_1} + e^{i\mathbf{k}.\delta_2} + e^{i\mathbf{k}.\delta_3}) \tag{1.2}$$

Here, the momentum vector $\mathbf{k}$ belongs to the first Brillouin zone of the graphene reciprocal lattice shown in Figure 1.3(b). $t = -2.7$ eV is the nearest-neighbor hopping potential. The bandstructure of graphene is shown in Figure 1.4.

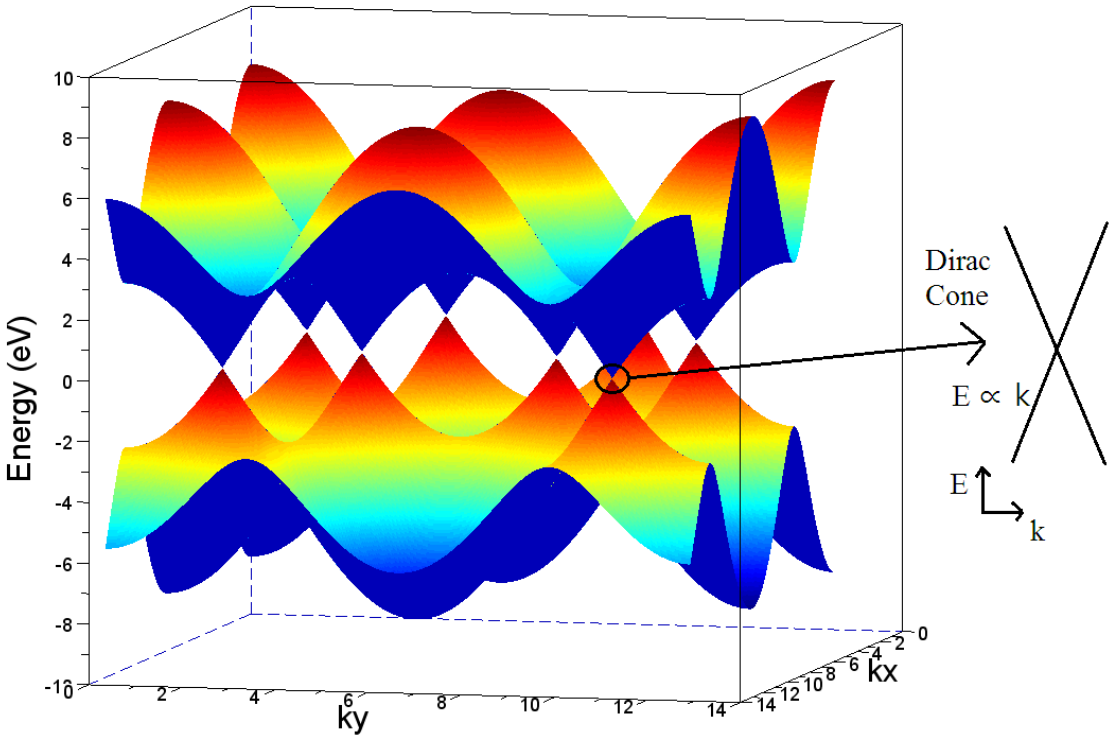


Figure 1.4: Bandstructure of graphene showing a representative Dirac cone

Graphene's bandstructure has "Dirac cones" at the **K** and **K'** points of the reciprocal lattice, where the energy spectrum is given by $E = \pm\nu_F\hbar\mathbf{k}$, where ν_F is the Fermi velocity and $\hbar$ is the reduced Planck's constant. The value of $\nu_F \approx 1.1 \times 10^8$ cm/s. Most of the electronic properties of graphene are determined by the nature of

the energy spectrum around these Dirac cones.

The energy spectrum of graphene around the high symmetry points is similar to the energy-momentum relationship for massless relativistic particles, albeit with a lower velocity of light (ν_F is analogous to the velocity of light for these particles in graphene). As a consequence, low energy Dirac fermions in graphene always move with a velocity that is independent of their energy and direction. This is responsible for the high carrier mobility of graphene [7].

Pristine graphene has its Fermi level at the point of intersection of the conduction and valence bands, called the Dirac point. The electronic density of states (DOS) at the Dirac point goes to zero. However, in the presence of a small electric field, the Fermi level is displaced to above or below the Dirac point, where the DOS varies linearly with energy. This is responsible for the ambipolar nature of graphene.

Like monolayer graphene, bilayer graphene also has interesting electronic properties. Bernal stacked bilayer graphene is a zero bandgap semiconductor, but with parabolic bands. With the application of a large interlayer field, a bandgap can be opened up as shown in Figure 1.5 [14].

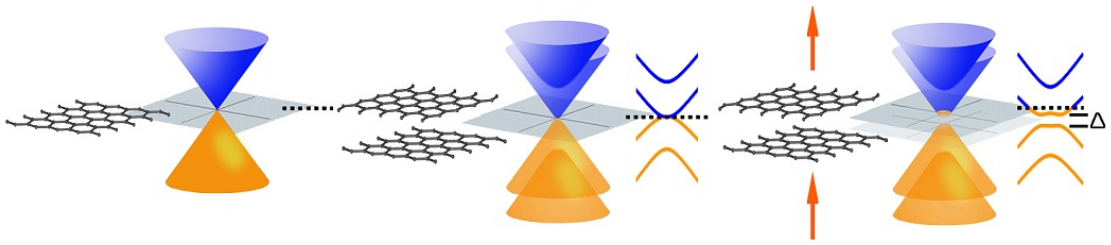


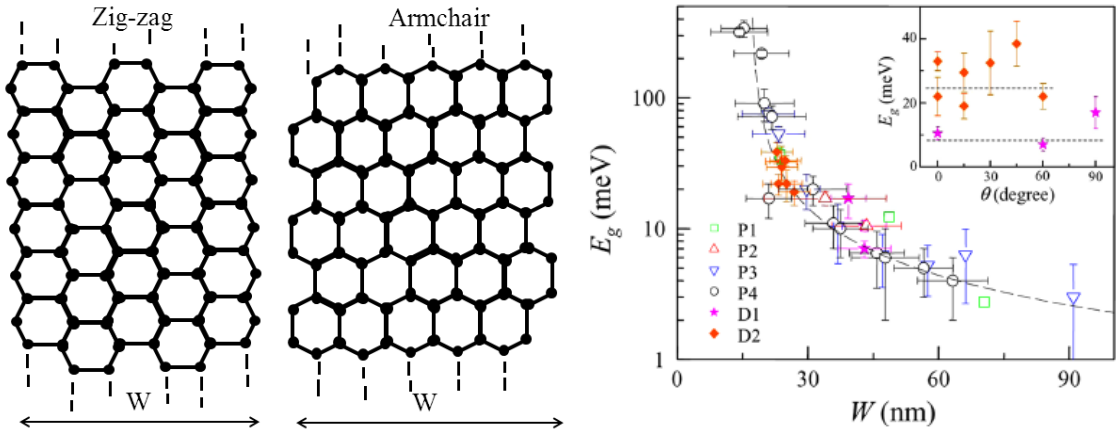
Figure 1.5: Electric-field-induced bandstructure asymmetry in bilayer graphene [14]

The electronic bandstructures of trilayer and multi-layer graphene are much more complicated. The bandstructure of multi-layer graphene converges rapidly with the number of layers and approaches the 3D limit of graphite at ten layers [15]. In general, once the number of graphene layers exceeds ten, it is no longer considered to

be graphene, but graphite.

Graphene Nanoribbons

While graphene's linear dispersion is responsible for the high carrier mobilities, the absence of a bandgap limits its use in conventional electronic devices. Bandgaps can however be opened up in monolayer graphene by confining it along one spatial dimension to form narrow strips of graphene called graphene nanoribbons (GNRs).



(a) Types of GNRs

(b) Bandgaps vs. GNR width

Figure 1.6: Graphene nanoribbons (GNRs) to open bandgaps in graphene [16]

Depending on the configuration of the carbon atoms on the graphene edge parallel to the length of the GNR, they are primarily classified as zig-zag or armchair (Figure 1.6(a)). Confinement along the width of the GNR leads to splitting of the original 2D dispersion of graphene into a number of 1D modes. The width and direction of confinement of the GNR determines its bandgap. Figure 1.6(b) shows experimental results of bandgaps of different GNRs with varying widths [16]. The bandgap is seen to empirically vary as the inverse of the GNR width.

The fabrication of GNRs is not straightforward and theoretical predictions indicate that their properties are a strong function of edge roughness [16].

Quantum Electrodynamics in graphene

Low energy electrons in graphene are accurately described by the relativistic version of the Schrödinger equation called the Dirac equation. These massless Dirac fermions can be seen as electrons that have lost their rest mass or as neutrinos that acquired the electron charge [6]. This makes it possible to probe quantum electrodynamics (QED) phenomena in graphene, often at room temperature.

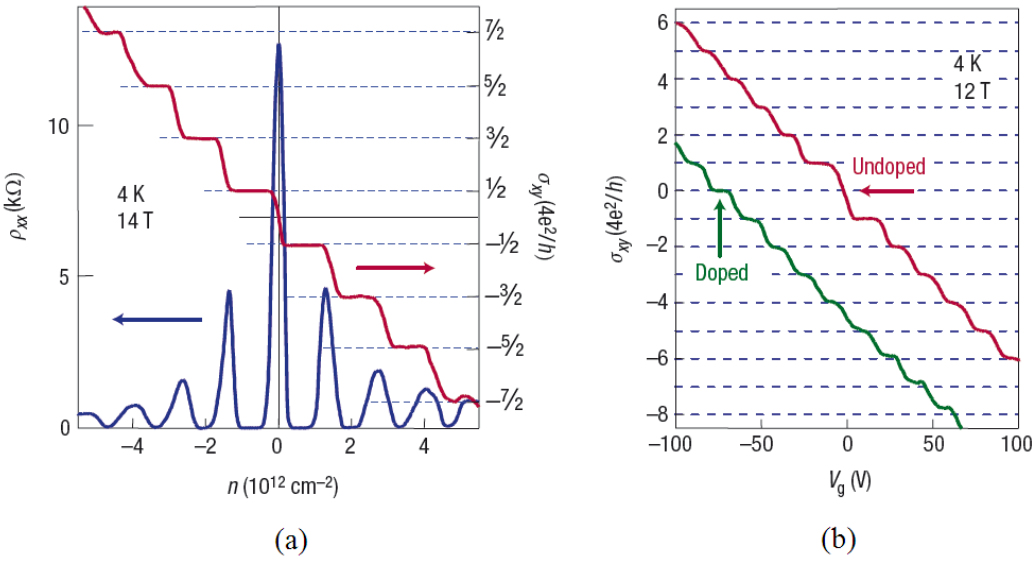


Figure 1.7: Quantum hall effect (QHE) in (a) monolayer graphene and (b) anomalous QHE in bilayer graphene [6]

Figure 1.7 shows experimental observation of (a) the quantum hall effect (QHE) in monolayer graphene and (b) anomalous QHE in bilayer graphene. QHE in monolayer graphene is a relativistic analogue of the integer QHE. The sequence is shifted with respect to the standard QHE sequence by 1/2. This is due to the existence of a quantized level at zero E, which is shared by electrons and holes.

The anomalous QHE in bilayer graphene manifests itself as a missing plateau at N = 0 in the Hall sequence. This is because electrons in bilayer graphene behave as chiral particles, but with a finite mass [6].

Doping of graphene

Pristine monolayer graphene without any impurities and in the absence of an electric field has its Fermi level passing through the Dirac point. In this "intrinsic" state, graphene has a zero DOS at its Fermi level and is expected to be an insulator. However, electron-hole puddles on the surface, due to impurities and disorder, lead to a finite resistance at the Dirac point [17].

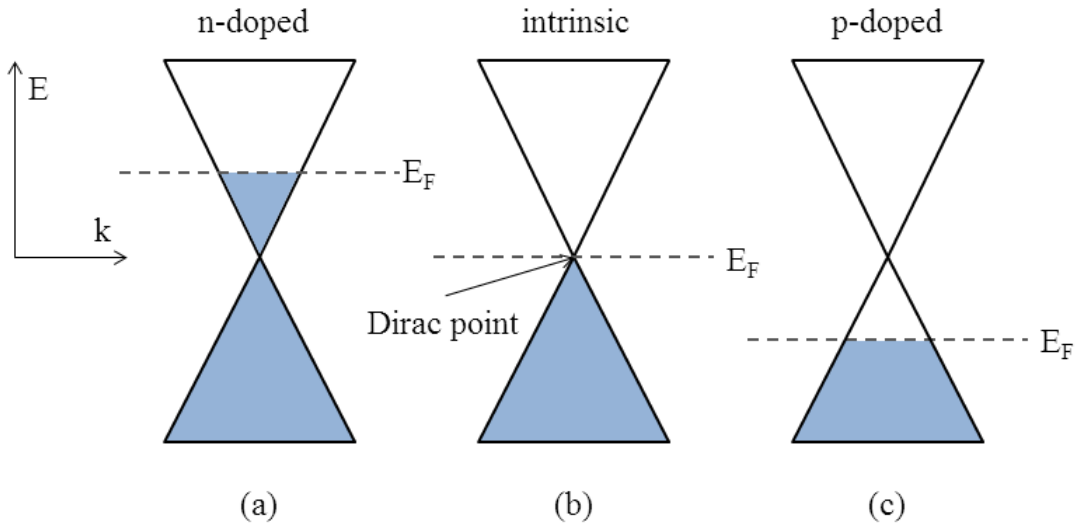


Figure 1.8: Positions of Fermi level in doped and intrinsic monolayer graphene

The position of the Fermi level in graphene can be modulated by an electric field effect using an FET structure [5]. A positive gate voltage shifts the Fermi level above the Dirac point and induces excess electrons and a negative gate voltage shifts it below the Dirac point and induces excess holes. Figure 1.8 shows the relative position of the Fermi level for doped and intrinsic graphene.

It is also possible to chemically dope graphene by substitutional or surface transfer doping [18]. Doping makes it possible to control the electronic properties of graphene and can also be used to open a bandgap [19]. Chemical doping of graphene is discussed in detail in Chapter 3.

1.4 Graphene: Synthesis

The ease of synthesis of a material is a major factor in deciding its adaptability to a large scale wafer integration process. For commercial viability, scalable large area synthesis of high quality graphene is essential.

The earliest attempts to isolate graphene from bulk graphite concentrated on chemical exfoliation, which involved separating graphene planes from graphite by intercalating them with a layer of intervening atoms or molecules [20]. This method was uncontrollable and had very low yield.

Method	**Scalability**	**Notes**
Micromechanical cleavage (exfoliation) [5]	Not scalable	Uses Scotch^{TM} tape to peel off graphene from graphite; high quality graphene; typically very small flakes ($\sim$ 100-1000 μm^2)
Epitaxial growth on SiC [21]	Scalable	Thermal decomposition of SiC to leave carbon atoms which form graphene; few-layer graphene possible; large area synthesis possible
CVD on Cu, Ni, Co films [22, 23, 24]	Scalable	CVD of carbon sources (methane, acetylene, etc.) on metal foils and films; need to be transferred; large area synthesis possible

Table 1.1: Approaches for obtaining mono- and few-layer graphene sheets

There have been many advances in graphene synthesis in the past few years. Table 1.1 summarizes the three major approaches used currently for obtaining high quality graphene.

While micromechanical cleavage is a very easy method for obtaining high quality mono- and few-layer graphene, it is not scalable and is used only for proof-of-concept demonstrations. SiC-epitaxy graphene and CVD graphene have a lower quality, but can be grown on a large scale.

Micromechanical cleavage: Exfoliation

Micromechanical cleavage was the first reported successful method of isolating monolayer graphene [5]. Highly oriented pyrolitic graphite (HOPG) or natural graphite is stuck to an adhesive tape and repeatedly peeled off using clean tape to successively thin it down. A clean Si/SiO_2 substrate is then attached to the tape and slowly peeled off, which causes a few graphene/graphite flakes to stick to it.

It is possible to detect the graphene layers optically on the substrate due to the subtle interference effects created by using a suitable thickness of SiO_2 (90 nm or 285 nm).

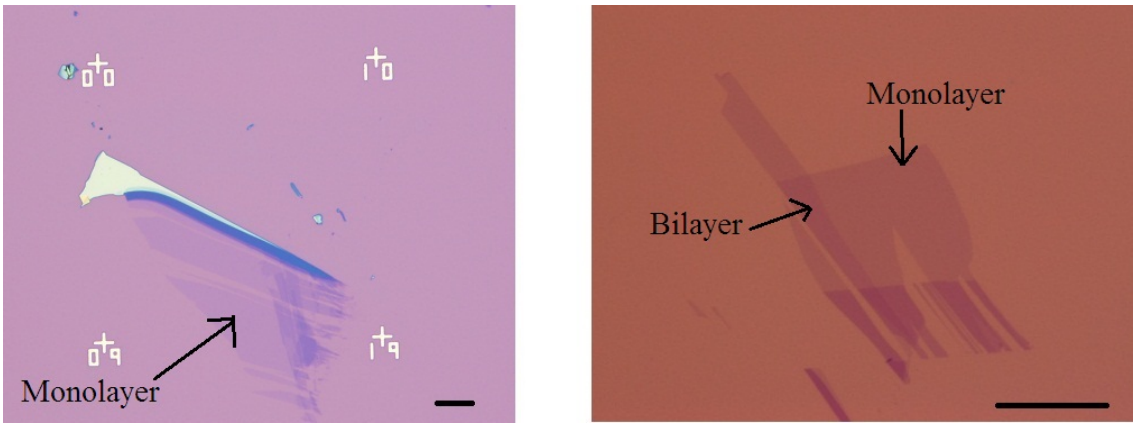


Figure 1.9: Exfoliated flakes on Si/SiO_2 (scale bars are 20μm)

Figure 1.9 shows exfoliated flakes on silicon substrates with 285 nm thermally grown SiO_2. Often, these flakes are accompanied by bilayer or multi-layer graphene regions nearby. Monolayers can be identified by their very slight optical contrast with respect to the substrate. Multi-layer graphene can be differentiated by its higher contrast.

Exfoliated graphene flakes occur in arbitrary shapes and arbitrary locations on the substrate, which makes this approach unsuitable for large scale production.

Epitaxial growth on SiC

Graphene can be grown epitaxially on SiC by heating the substrate to near 1200°C in an ultra-high vacuum chamber. This leads to desorption of silicon from the surface and causes the remaining carbon atoms to form a graphene layer. This is a repetitive process and can be used to grow multi-layer graphene depending on the growth time and temperature. The first graphene layer is a buffer layer which is directly bonded to the substrate. This layer does not show a Dirac spectrum. Layers above the first layer behave like monolayer graphene [21].

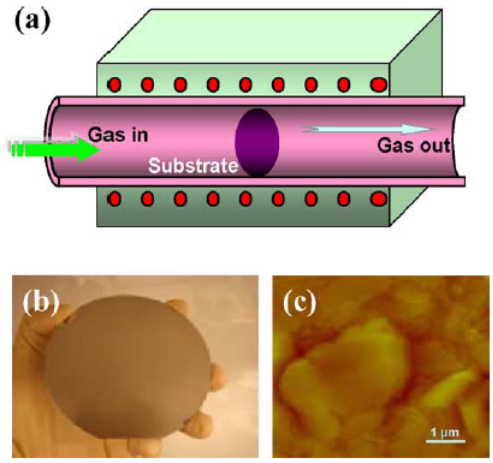
SiC has two types of surfaces - a Si-terminated one and a C-terminated one. The quality and number of graphene layers grown depend on the face used for growth. It turns out that graphene grown on the Si-terminated face has lower mobilities than graphene grown on the C-terminated face.

Epitaxial growth requires ultra-high vacuum conditions which are not easy to attain. Theoretically it is possible to start with a wafer of SiC and end with an entire wafer of graphene. But SiC is very expensive and hence SiC-epitaxy is not the best option for large scale graphene growth.

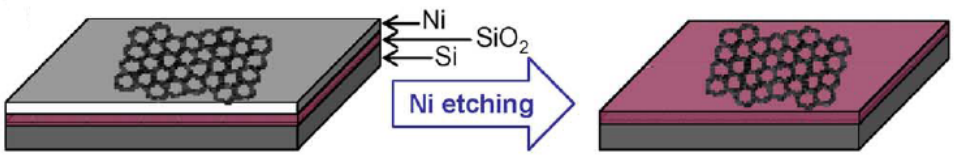
Chemical vapor deposition (CVD)

Chemical vapor deposition (CVD) growth of graphene is done by decomposing carbon precursors on transition metal substrates like Cu, Ni and Co. Typical carbon precursors include hydrocarbons like methane, acetylene, hexane, benzene, etc. The metal substrate is in the form of a metal foil or a Si/SiO_2 substrate coated with a thin film of the transition metal.

The metal substrate is heated to around 1000°C and a carbon precursor is flown over it. The hydrocarbon decomposes on the metal surface and some carbon gets



(a) Schematic of the CVD furnace, (b) optical micrograph and (c) AFM image of the grown graphene



(b) Schematic of the transfer process

Figure 1.10: Schematics of graphene growth by CVD on Ni films [25]

dissolved in it. On cooling the substrate, the dissolved carbon segregates on the surface as graphene [22]. Figure 1.10 shows schematic images of CVD graphene growth on Ni films [25].

Graphene is then transferred to the substrate of interest using a PMMA or a PDMS transfer layer after etching away the metal film [24]. CVD grown graphene has lower mobilities than exfoliated graphene, but it can be grown on a wafer-scale. The graphene is also not one single crystal, but is made out of multiple grains originating at the grain boundaries of the metal film used for growth.

CVD graphene seems to be the most promising method of graphene synthesis for commercial viability, owing to its compatibility with CMOS processes.

1.5 Thesis organization

Graphene is a promising material for post-CMOS devices due to its exciting electronic properties and scaling potential. Graphene field effect transistors (GFETs) have the potential to replace conventional Si MOSFETs. This thesis presents a method of improving GFET performance by doping their source/drain access regions with surface transfer dopants in a self-aligned manner.

Chapter 2 focuses on fabrication and electrical measurements of GFETs. Methods of characterizing and identifying monolayer graphene and subsequent processing steps for fabricating back-gated and top-gated GFETs are described. An analytical model of transistor operation is presented which can be used to extract carrier mobilities. Electrical measurements of back-gated and top-gated GFETs are presented and are fitted to the model to extract mobilities. The effect of unintentional doping of graphene during fabrication and hysteresis in electrical measurements of GFETs are touched upon.

Methods of doping graphene and techniques of characterizing doped graphene are elaborated on in Chapter 3. A summary of literature reports of substitutional and surface transfer doping of graphene is presented. Experimental results of organic surface transfer doping of graphene using poly(methyl methacrylate) (PMMA), tetracyanoquinodimethane (TCNQ) and poly(ethylene imine) (PEI) are discussed. Raman spectroscopy and electrical transport measurements are used to characterize doped graphene. The chapter concludes with a section on doping loss and methods of preventing doping loss by sealing the dopants using a capping layer.

Chapter 4 extends the methods of doping graphene presented in Chapter 3 to the source/drain access regions of top-gated GFETs to improve their performance. The motivation behind self-aligned transistors is given and a review of previous attempts

at self-aligned GFET fabrication are outlined. A novel method of spin-on-doping graphene using PEI as a dopant is developed and is employed to dope the source/drain access regions of top-gated GFETs. An overview of the fabrication process-flow is given along with electrical measurements after every major processing step, showing an improvement in GFET performance after self-aligned doping. Fabrication of GFETs on quartz and their advantages are discussed. GFETs on quartz are finally self-aligned doped and their performance enhancements are presented.

Chapter 5 presents a summary of the work and suggests some possible future research directions.

2

Graphene Field-Effect Transistors

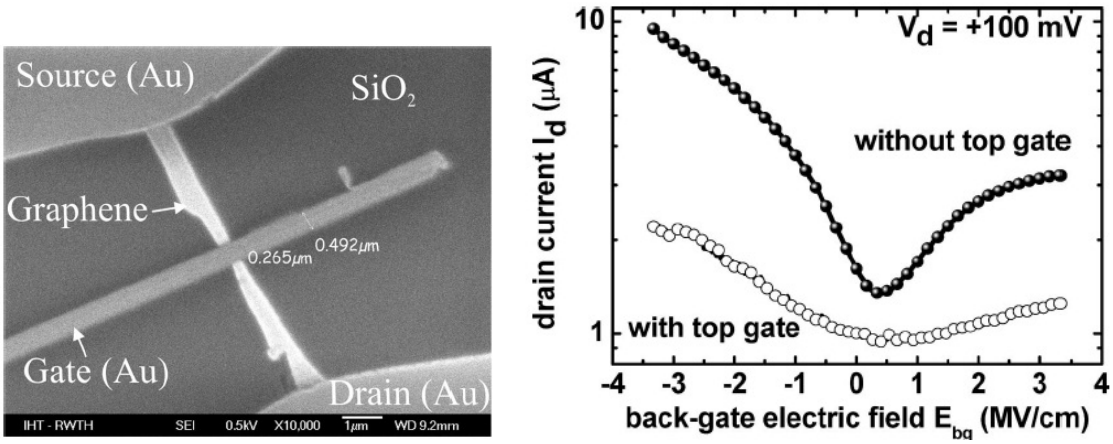
The basic topology of any field effect transistor (FET) consists of a semiconductor channel material, source and drain electrodes for current injection and a gate electrode and gate dielectric to modulate this current by electric field action. Graphene FETs (GFETs) are FETs with graphene as the channel material. GFETs are considered promising devices for post-CMOS electronics owing to graphene's high mobility and ultra-thin nature. This chapter describes fabrication of back-gated and top-gated GFETs and their electrical characteristics.

2.1 GFETs from literature

The first GFETs were fabricated using few-layer exfoliated graphene on glass slides using contacts made of silver paste [26]. The first formal demonstration of a GFET was a back-gated FET on monolayer graphene with a heavily doped Si back-gate and 300 nm SiO_2 gate dielectric [5]. Back-gated devices are good for proof of concept but cannot be used for realistic applications due to large parasitic capacitances and poor gate control [13].

A top-gated GFET is like a conventional Si MOSFET, but with graphene as the channel material. These top-gated GFETs are typically fabricated on heavily doped Si/SiO_2 substrates which makes it possible to modulate their channel resistance using the back-gate as well. This allows for dual-gating of the graphene and these devices are also referred to as dual-gated GFETs.

The first top-gated GFET used evaporated SiO_2 as the top-gate dielectric and was fabricated on exfoliated graphene [27]. It showed mobilities higher than conventional Si MOSFETs (710 cm^2/Vs for holes and 530 cm^2/Vs for electrons). Figure 2.1 shows an SEM image and the transfer characteristics of the first top-gated GFET [27].



(a) SEM image of the GFET

(b) I_d-E_{bg} of the GFET

Figure 2.1: SEM image and transfer characteristics of the first top-gated GFET [27]

Top-gated GFETs have been fabricated using a variety of top-gate dielectrics such as Al_2O_3, HfO_2, SiO_2, etc [27, 28, 29]. GFETs fabricated on exfoliated graphene, SiC epitaxially grown graphene and CVD graphene have also been reported [28, 29, 22, 30]. GFETs have also been fabricated on flexible substrates like polyimide films and insulating substrates like quartz [31, 30]. Bilayer GFETs use bilayer graphene as the channel material since a band-gap can be opened in bilayer graphene [32]. GFETs on hexagonal Boron Nitride (h-BN) substrates and GFETs using h-BN as

the top-gate dielectric have also been fabricated and show high mobilities due to the complementary 2D nature of h-BN [33, 32]. Table 2.1 gives a summary of various top-gated GFETs reported in literature.

Work	**Graphene Source**	**Notes**
M. C. Lemme *et. al.* [27]	Exfoliated monolayer	Evaporated SiO_2 dielectric; hole mobility of 710 cm^2/Vs and electron mobility of 530 cm^2/Vs
Y. M. Lin *et. al.* [29]	1-2 layer on SiC	ALD HfO_2 dielectric; mobilities from 900 to 1500 cm^2/Vs; 100 GHz f_T
S. Kim *et. al.* [28]	Exfoliated monolayer	ALD Al_2O_3 with Al seed layer; field-effect mobility 8000 cm^2/Vs
X. Li *et. al.* [22]	Cu CVD monolayer	ALD Al_2O_3 with Al seed layer; field-effect mobility 4000 cm^2/Vs
I. Meric *et. al.* [33]	Exfoliated monolayer	Exfoliated h-BN gate dielectric; hole mobility of 10,000 cm^2/Vs and electron mobility of 8,600 cm^2/Vs
H. Wang *et. al.* [32]	Exfoliated bilayer	Bilayer sandwiched by h-BN as substrate and dielectric; Hall mobility of 15,000 cm^2/Vs; f_T = 33 GHz
J. Lee *et. al.* [31]	Cu CVD monolayer	Monolayer graphene on flexible substrates; ALD Al_2O_3; field-effect mobility of 5,000 cm^2/Vs
M. Ramon *et. al.* [30]	Cu CVD monolayer	Monolayer graphene on quartz substrates; ALD Al_2O_3; field-effect mobility of 5,000 cm^2/Vs

Table 2.1: Top-gated GFETs from literature

GFETs have poor ON/OFF ratios because of the absence of a bandgap in graphene. Poor ON/OFF ratios coupled with the absence of a saturation region in the output characteristics makes GFETs unsuitable for logic applications [13]. However, the merit of GFETs over conventional Si MOSFETs is their high carrier mobilities, the scope for scalability due to graphene's ultra-thin body and its ambipolar nature of conduction. This facilitates the use of GFETs for analog and high performance radio frequency (RF) applications [29, 30, 34].

2.2 Fabrication of GFETs

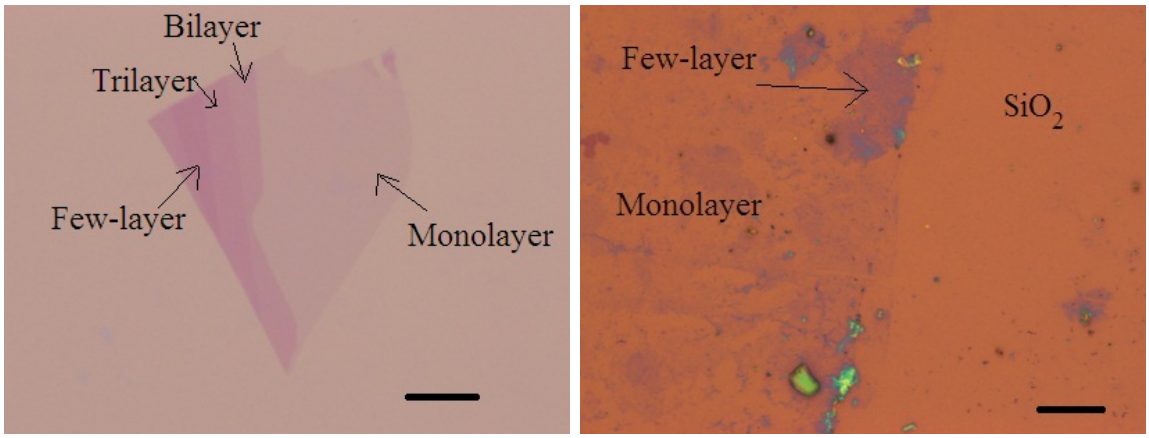
Fabrication of GFETs involves synthesis and characterization of graphene, deposition of metal contacts to make a back-gated device and subsequent top-gate dielectric deposition followed by top-gate metal deposition to make a top-gated device.

2.2.1 Graphene Characterization

It is essential to identify and distinguish between monolayer, bilayer and few-layer graphene in order to fabricate a GFET using the right type of graphene. Methods of characterizing graphene before fabricating a GFET device are presented here.

Optical Identification

Monolayer, bilayer, trilayer and few-layer graphene can be distinguished from each other on a Si/SiO_2 substrate with the right thickness of SiO_2 (90 nm or 300 nm) due to optical interference effects between the graphene and SiO_2 [35].



(a) Exfoliated graphene (b) CVD grown graphene

Figure 2.2: Optical micrographs of graphene showing optical contrast with the substrate (scale bars are 10μm)

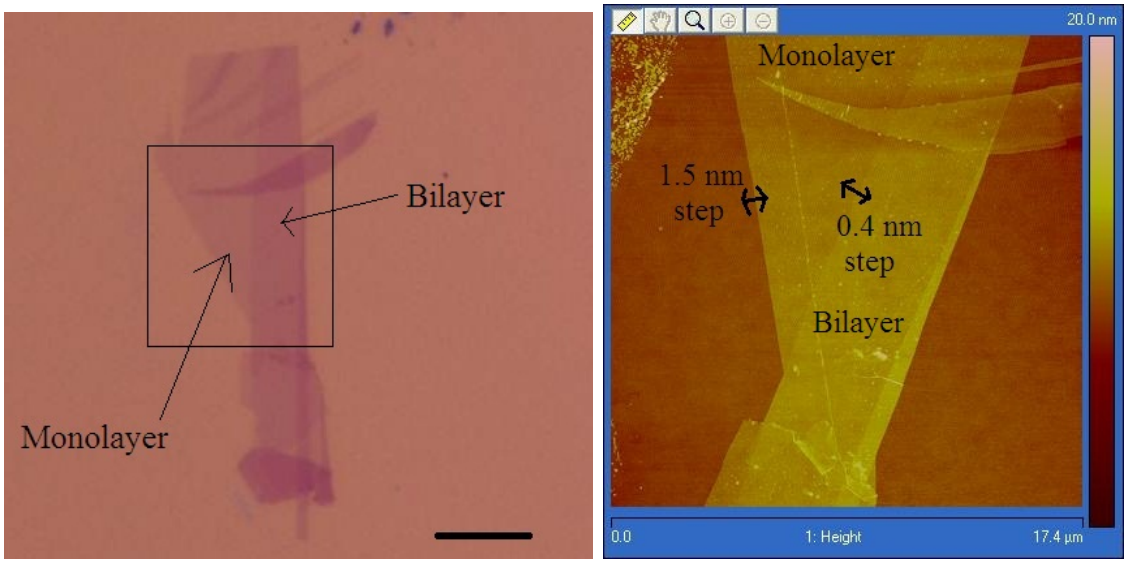
Figure 2.2(a) shows the optical micrograph of an exfoliated graphene flake and

Figure 2.2(b) of a CVD grown graphene film on a 300 nm SiO_2-on-Si substrate. The thickness of the underlying SiO_2 layer is very critical and even a small (5%) mismatch could drastically reduce the contrast making it difficult to see monolayer graphene [35].

The contrast of graphene increases with the number of layers and it is possible to identify the number of layers from optical contrast alone. The use of color filters further enhances or diminishes this contrast depending on the SiO_2 thickness [35]. Identification of graphene by optical contrast requires a trained eye and can be an easy and powerful method of graphene characterization.

Atomic force microscopy (AFM)

Atomic force microscopy (AFM) can be directly used to measure the thickness of graphene films. The value of interlayer spacing in graphite (0.34 $\AA$) can then be used to calculate the number of graphene layers.



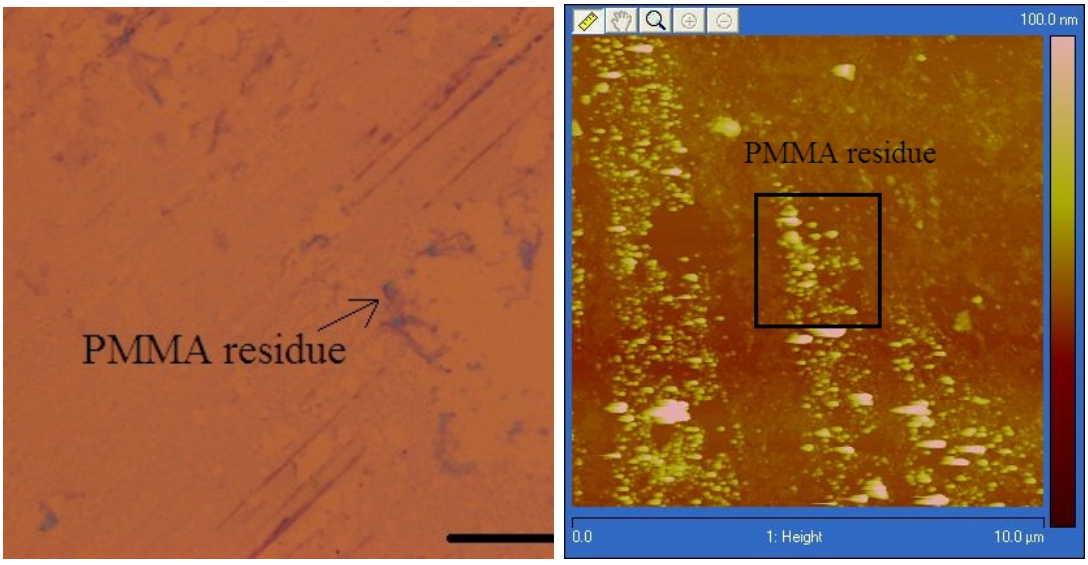
(a) Optical micrograph (scale bar is 10μm) (b) AFM scan of boxed region

Figure 2.3: Optical micrograph and AFM scan of a graphene flake

Figure 2.3(a) shows the optical micrograph of a graphene flake whose AFM scan is shown in Figure 2.3(b). The scan was taken with the AFM operating in the tapping-mode. Monolayer graphene shows a step height of around 1.5 nm on a SiO_2 substrate, which is higher than what is expected.

This could be because of two reasons: (1) a difference in interaction force between the tip and graphene compared to the tip and the substrate. This causes an instrumental height offset of around 1 nm between graphene and the substrate [36]. And (2) because of an adsorbed layer of hydrocarbons or water on the graphene or at the graphene-substrate interface [5].

AFM is also a powerful tool to detect PMMA residues on CVD grown graphene. These residues are often not visible on optical micrographs, but show up on AFM scans. Figure 2.4(b) shows the AFM scan (with PMMA residues highlighted in a box) of CVD graphene (optical micrograph shown in Figure 2.4(a)).



(a) Optical micrograph (scale bar is 10μm) (b) AFM scan showing PMMA residue

Figure 2.4: Optical micrograph and AFM scan of CVD grown graphene

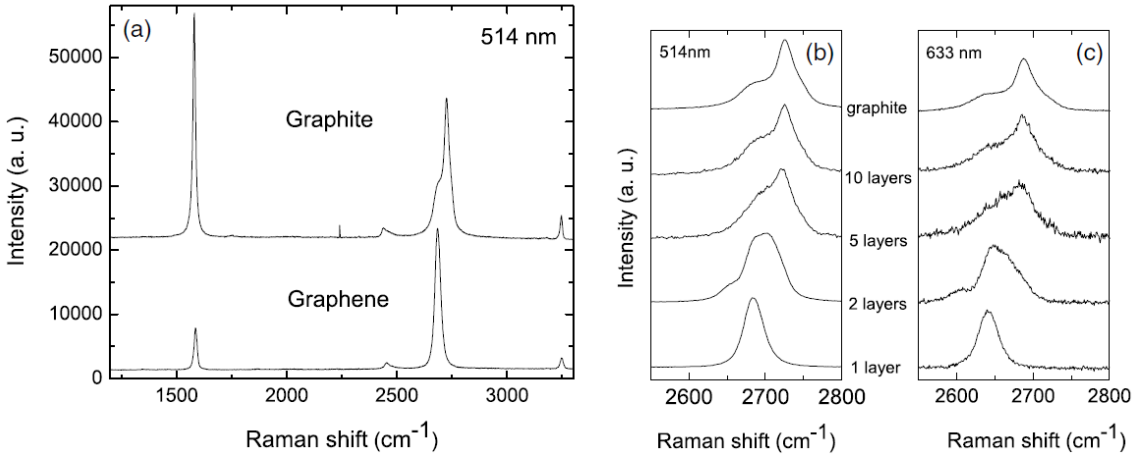
AFM tips can sometimes destroy graphene films by peeling them off the substrate.

The force with which the tip scans the surface needs to be kept as low as possible to minimize the risk of tearing and ripping graphene. AFM scanning of graphene thus needs to be done with extreme care and is avoided unless there is a need to check roughness of the films.

Raman spectroscopy

The Raman spectrum of a solid contains information about its vibrational and electronic properties. The electronic structure of graphene is uniquely captured in its Raman spectrum and evolves with the number of layers [37]. Raman spectra can hence be used to identify the number of graphene layers.

All graphite systems have two distinct peaks in their Raman spectrum - the G peak at ~ 1580 cm^{-1} and the G' (2D) peak at ~ 2700 cm^{-1}. The G peak is due to the doubly degenerate zone center E_{2g} mode [37]. The 2D peak is the second order of zone-boundary phonons. Figure 2.5(a) shows the Raman spectra of monolayer graphene and graphite [37].



(a) Raman spectra of graphene and graphite

(b) Evolution of the 2D peak with number of graphene layers

Figure 2.5: Raman spectra of few-layer graphene [37]

The shape of the 2D peak, its full-width at half maximum (FWHM) and the ratio of heights of the 2D to the G peaks are directly related to the number of graphene layers (Figure 2.5(b)). Monolayer graphene has a single sharp 2D peak with a FWHM ~ 25 cm^{-1}. Bernal stacked bilayer graphene has a broad 2D peak and the G peak is higher than the 2D peak.

Few-layer graphene and graphite show a distinct shoulder on the 2D peak. The ratio of the height of the G peak to the 2D peak also increases with the number of graphene layers. The Graphene with defects in the basal plane gives a peak at ~ 1350 cm^{-1} called the D peak. Raman spectra of exfoliated monolayer, bilayer, defected monolayer graphene flakes and bulk graphite are shown in Figure 2.6.

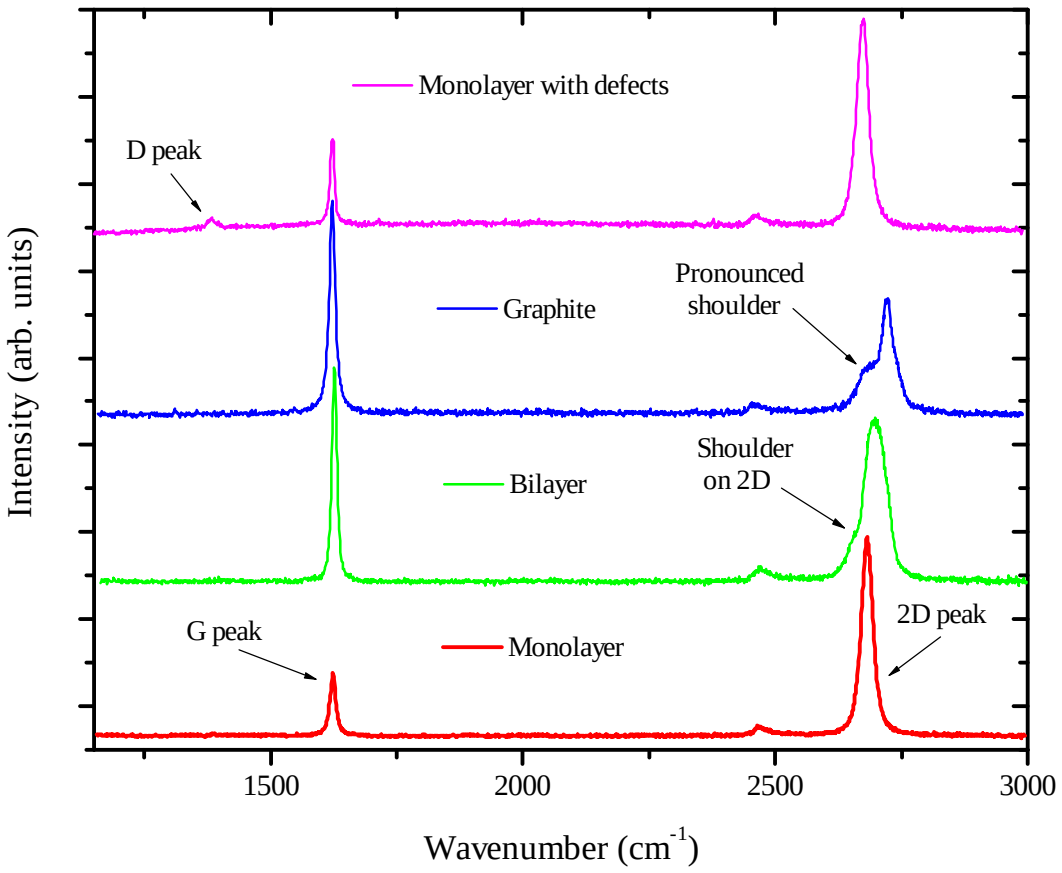


Figure 2.6: Raman spectra of various graphene samples

2.2.2 Back-gated GFETs

A back-gated GFET uses a highly doped Si wafer as the back-gate. The back-gate dielectric is an SiO_2 layer. To this end, highly-doped n-type Si (100) wafers with an arsenic doping concentration of $N_D > 10^{20}/cm^3$ were used as the substrate. A 300 nm layer of SiO_2 was grown using dry oxidation at 1050°C. Alignment markers were patterned using optical lithography and 5 nm Cr/ 25 nm Pt deposition. These alignment markers are used for tracking flakes on the substrate and for alignment during e-beam lithography (EBL).

Graphene was exfoliated onto these substrates using the micromechanical cleavage (scotch-tape) method described in Chapter 1. Monolayer graphene flakes were identified using optical contrast under an optical microscope and confirmed using Raman spectroscopy. As-exfoliated graphene flakes are typically attached to much thicker regions of graphene on the side and are often irregularly shaped.

These irregularly shaped graphene flakes were patterned to a regular rectangular shape using e-beam lithography (EBL) with 4% PMMA as the e-beam resist. Extra graphene was etched away using an oxygen plasma etch for 30 - 60 s. The substrate was then re-coated with a fresh layer of PMMA for metal contact patterning.

Source and drain contacts (or 4-point Hall-bar structures) were patterned using EBL and a 50 nm layer of Ni was deposited using e-beam evaporation. The substrate was then left in acetone for 24 hours to finish the lift-off process and finish fabrication of the back-gated GFET.

Figure 2.7 shows a schematic of the fabrication process-flow for back-gated GFETs. This specific flow is for a GFET differential pair on the same graphene flake. This device has one source electrode and two drain electrodes, forming a symmetric differential pair. The fabrication process-flow for CVD graphene based GFETs is identical.

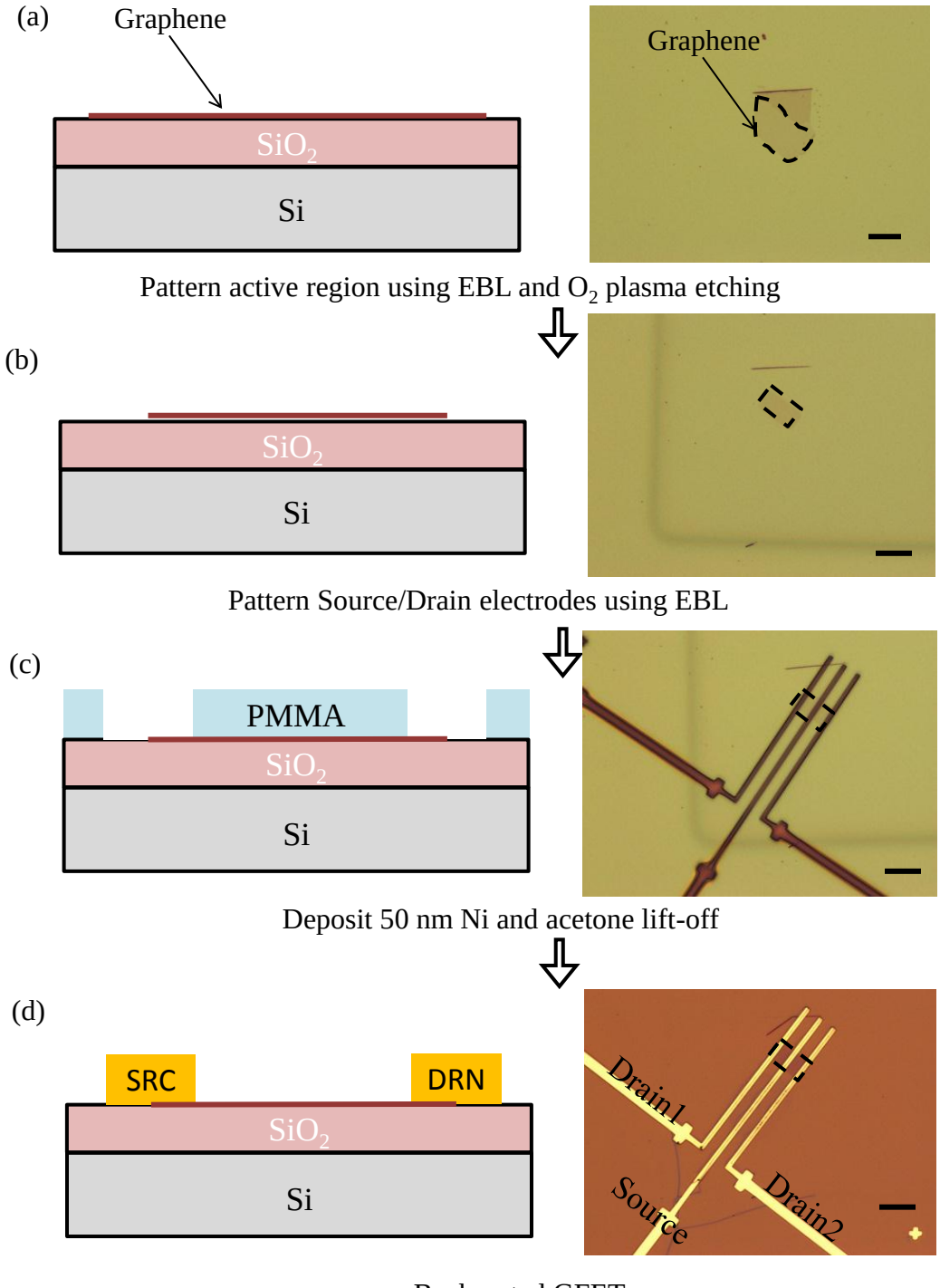


Figure 2.7: Schematic showing fabrication process-flow of back-gated GFETs. Optical micrographs at each step are shown on the right (all scale bars are 10μm)

2.2.3 Top-gated GFETs

Back-gated GFETs do not allow independent control of multiple devices on the same substrate because they all share a common back-gate. Top-gated GFETs offer independent control and also have better device characteristics owing to smaller parasitic capacitances [13].

The challenge in fabricating top-gated GFETs is the deposition of a top-gate dielectric on graphene. Evaporated SiO_2 is an option, but this degrades the mobility of graphene [27]. Several high-κ dielectrics (like Al_2O_3, HfO_2, etc.) can be deposited using atomic layer deposition (ALD), but the chemically inert basal plane of graphene with the absence of dangling bonds makes it impossible to do ALD on graphene [28].

The way out of this is to deposit a seed layer on graphene before ALD. A thin $15\mathring{A}$ layer of Al was deposited on the back-gated GFET using e-beam evaporation. Once the sample is brought out into ambient, this layer oxidizes and forms Al_2O_3 [28]. ALD was then performed with the oxidized seed layer providing nucleation centers for ALD growth. The ALD growth was done at 250°C using alternating cycles of water (H_2O) and Tri-methyl Aluminum ($Al(CH_3)_3$) precursors.

The top-gate electrode is then patterned using EBL and 50 nm Ni deposited for the top-gate metal contact followed by an acetone lift-off process. The source/drain metal pads have ALD Al_2O_3 on them which needs to be etched off before electrical measurements can be made on the GFET. This is done using a 1:50 dilute HF solution after patterning the metal pad windows in a separate EBL step.

Figure 2.8 shows a schematic of the fabrication process-flow for a top-gated GFET starting from a back-gated GFET. This flow is a continuation of the flow shown in Figure 2.7 to fabricate a differential GFET pair. The completed device has two symmetric top-gated GFETs with a shared source electrode.

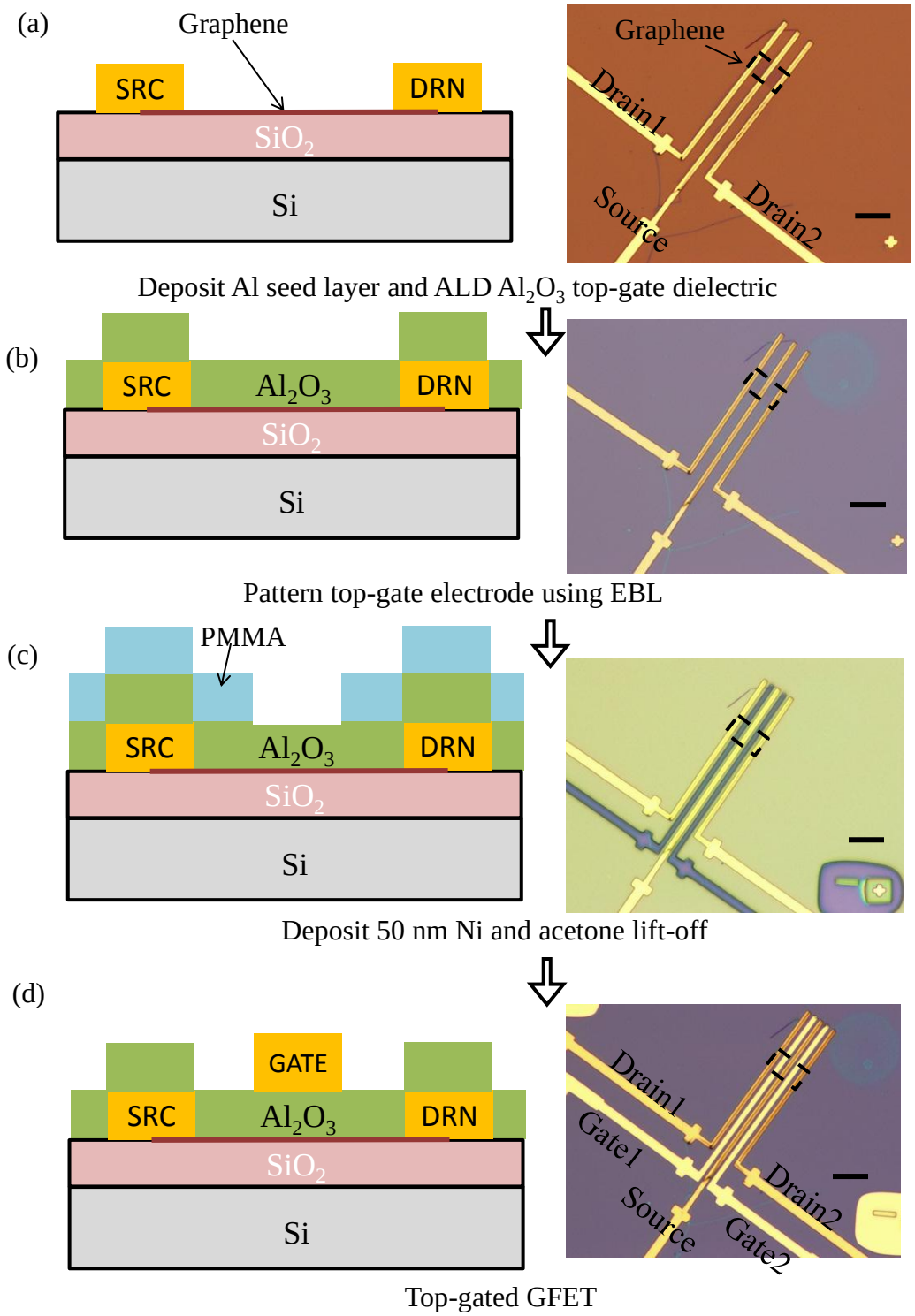


Figure 2.8: Schematic showing fabrication process-flow of top-gated GFETs. Optical micrographs at each step are shown on the right (all scale bars are 10μm)

2.3 GFET modeling

Many intrinsic properties of graphene cannot be directly measured, but need to be extracted from experimental data by fitting to a model. The carrier mobility and residual carrier concentration are two such properties that can be extracted from the electrical measurements of a GFET.

Applying a top-gate voltage modulates the carrier concentration in graphene. This changes its resistance and gives rise to transistor action. Figure 2.9 shows the schematic of a top-gated GFET with the resistance and capacitance components which need to be included in the model. R_G is the graphene channel resistance, R_C the contact resistance at the source and drain ends, C_{TG} is the top-gate capacitance and C_q is the quantum capacitance of graphene.

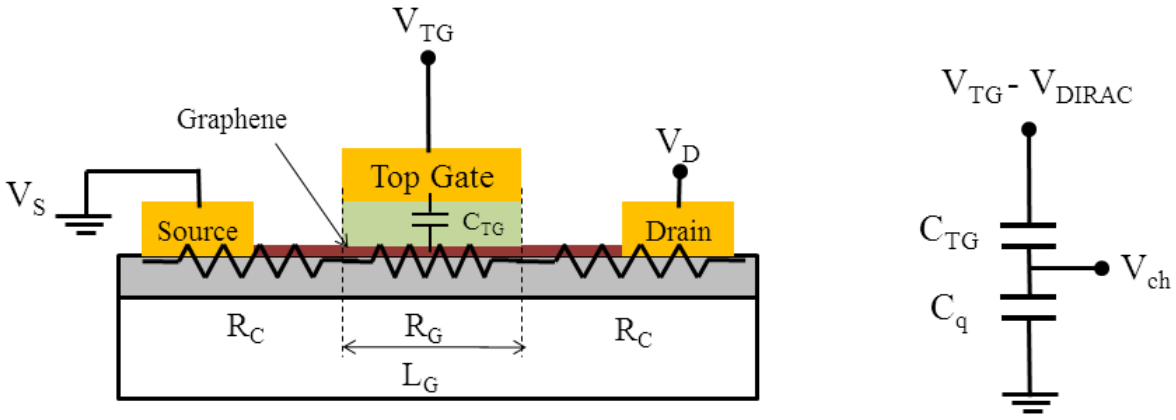


Figure 2.9: Schematic of resistances in a top-gated GFET

The carrier concentration in the graphene channel region (n_{tot}) can be written using Equation 2.1 [28].

$$n_{tot} = \sqrt{{n_0}^2 + n({V_{TG}}^*)^2} \tag{2.1}$$

Here, n_0 represents the residual carrier concentration [38]. $n({V_{TG}}^*)$ represents the carrier concentration induced by the top-gate away from the Dirac point. ${V_{TG}}^* = V_{TG} - V_{DIRAC}$ is the effective top-gate bias referred to the Dirac point. Ideally, the Dirac point is expected to be at 0 V, but unintentional doping during the fabrication process could give rise to a non-zero V_{DIRAC} and hence needs to be accounted for in the model.

The expression for $n({V_{TG}}^*)$ is given by Equation 2.2, where e is the electron charge and $\hbar$ is the reduced Planck's constant.

$$ {V_{TG}}^* = \frac{e n_{tot}}{C_{TG}} + \frac{\hbar \nu_F \sqrt{\pi n_{tot}}}{e} \tag{2.2} $$

Assuming a Drude model for the carrier mobility μ, the total resistance of the GFET operating under a small drain bias (V_D) can then be written using Equation 2.3 [28].

$$ R_{tot} = 2R_C + R_G = 2R_C + \frac{N_\square}{n_{tot} e \mu} \tag{2.3} $$

Here, $N_\square$ is the number of squares in the channel region and is given by $N_\square = L_G/W_G$, where L_G and W_G are the length and width of the graphene channel region.

This model can be used to extract carrier mobilities and residual carrier concentrations of graphene from electrical measurements. Often, contact resistance is unknown and can be extracted too. The effect of contact resistance can be nullified by taking 4-point measurements using a Kelvin resistance contact scheme.

The same model can be used to extract mobilities of back-gated devices by replacing the top-gate voltage with the back-gate voltage. Extracted μ and n_0 values from this model match well with those from graphene transport models in the diffusive limit using Boltzmann transport formalism [38].

2.4 Electrical measurements

Electrical measurements of GFETs were made on a probe station under ambient conditions at room temperature. Most of the back-gated GFETs had 4-point probe structures for resistance measurement as a function of the back-gate voltage (V_{BG}). A small drain bias (typically 20 mV) was applied, with the source electrode grounded. The voltage between the voltage measurements probes was measured and divided by the current flowing through the device to get the channel resistance. Figure 2.10 shows the 4-point resistance measurements of a back-gated GFET ($W_G/L_G = 5.0\mu m/12.0\mu m$) as a function of V_{BG}.

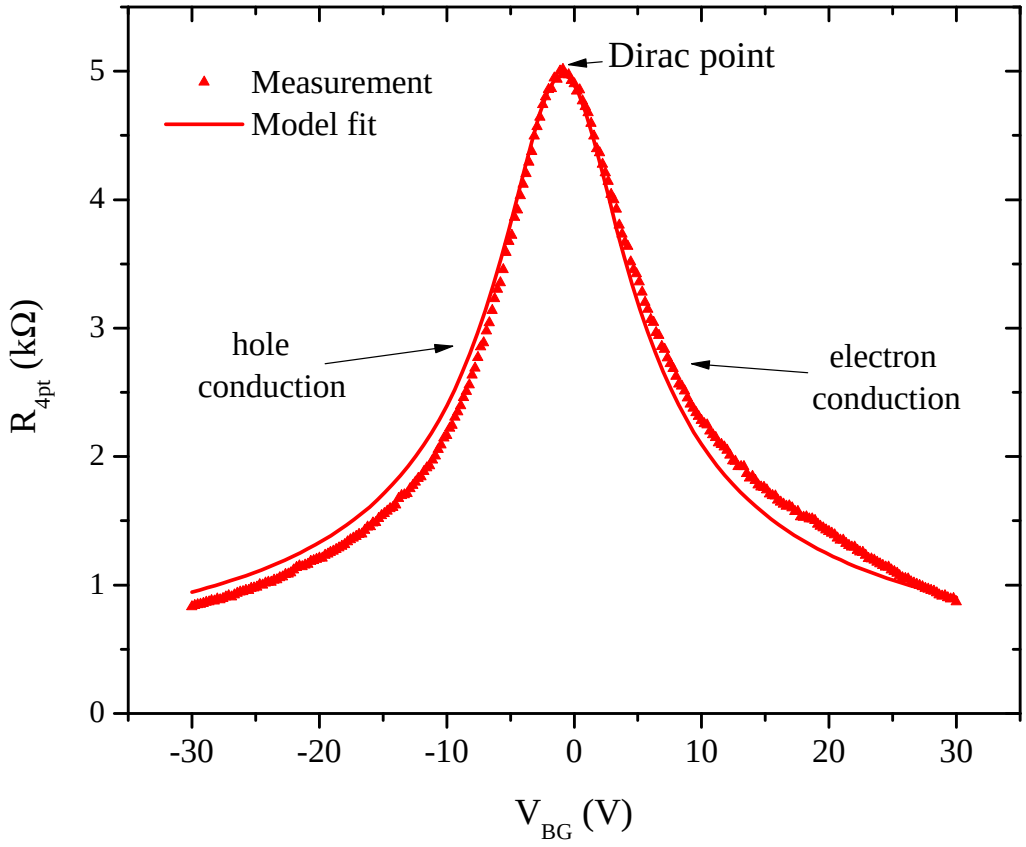


Figure 2.10: 4-point resistance vs. V_{BG} at $V_D = 20$ mV on a back-gated GFET

The familiar Λ shaped curve is seen with the Dirac point close to 0 V which

suggests very little unintentional doping [5]. Fitting the experimentally measured values to the model gives a carrier mobility of 9,400 cm^2/Vs with a residual carrier concentration of $3\times10^{11}/cm^2$.

2.4.1 Doping

Typical back-gated GFETs do not have their Dirac point at 0 V, but are unintentionally doped to either a positive or a negative Dirac voltage. This unintentional doping could be due to adsorbed water and gas molecules or due to impurities from the fabrication process [19]. Figure 2.11 shows 4-point resistance measurements of three different as-fabricated back-gated GFETs, each with a different level of unintentional doping.

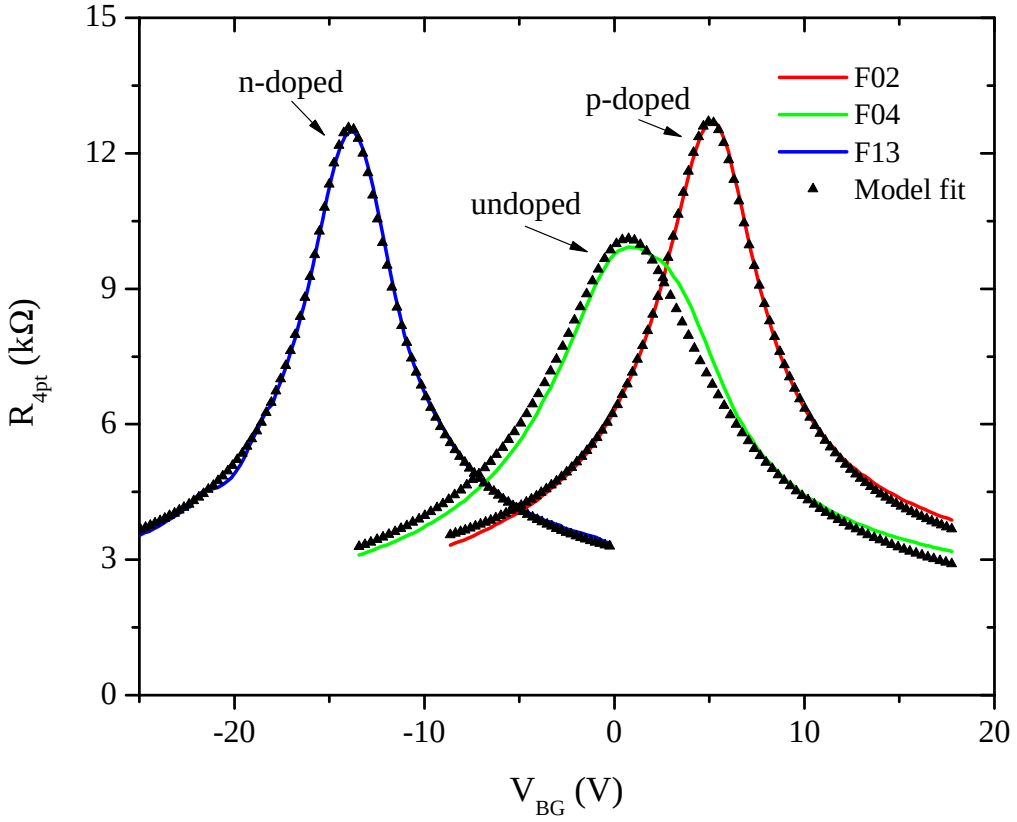


Figure 2.11: 4-point resistance of unintentionally doped GFETs F02, F04 and F13

Doping shifts the Dirac point to a positive (p-doped) or negative (n-doped) voltage. For example, n-doped graphene has its Fermi level above the Dirac point and has excess electrons in the graphene channel at zero V_{BG}. On application of a sufficiently large negative voltage, these excess electrons get depleted and the Fermi level moves to the Dirac point. This is the reason for the negative Dirac voltage of n-doped graphene. In analogy, p-doped graphene has a positive Dirac voltage.

The amount of doping can be calculated from the Dirac voltage using Equation 2.4. Here, C is the gate capacitance, V_{DIRAC} is the Dirac voltage and e the electron charge.

$$n_{dopant} = \frac{CV_{DIRAC}}{e} \tag{2.4}$$

The extracted mobility values are: F02: 3,800 cm^2/Vs, F04: 5,200 cm^2/Vs and F13: 3,900 cm^2/Vs. The doping concentrations are: F02: $3.43\times10^{11}/cm^2$ (holes), F04: $6\times10^{9}/cm^2$ (holes) and F13: $9.68\times10^{11}/cm^2$ (electrons).

Graphene can also be intentionally doped using substitutional dopants and surface transfer dopants. Methods of doping graphene are discussed in Chapter 3.

2.4.2 Hysteresis

Hysteretic behaviors are often observed in the conductance characteristics of back-gated GFETs. The hysteresis varies depends on the back-gate voltage sweeping range, the sweeping rate and adsorbed species on the graphene. Adsorbed polar molecules like water are majorly responsible for hysteresis [39].

Figure 2.12 shows the effect of the back-gate voltage sweeping rate on hysteresis in the resistance profile of a back-gated GFET being tested under ambient conditions. A high back-gate voltage sweep rate results in a low hysteresis and a low back-gate voltage sweep rate in a large hysteresis.

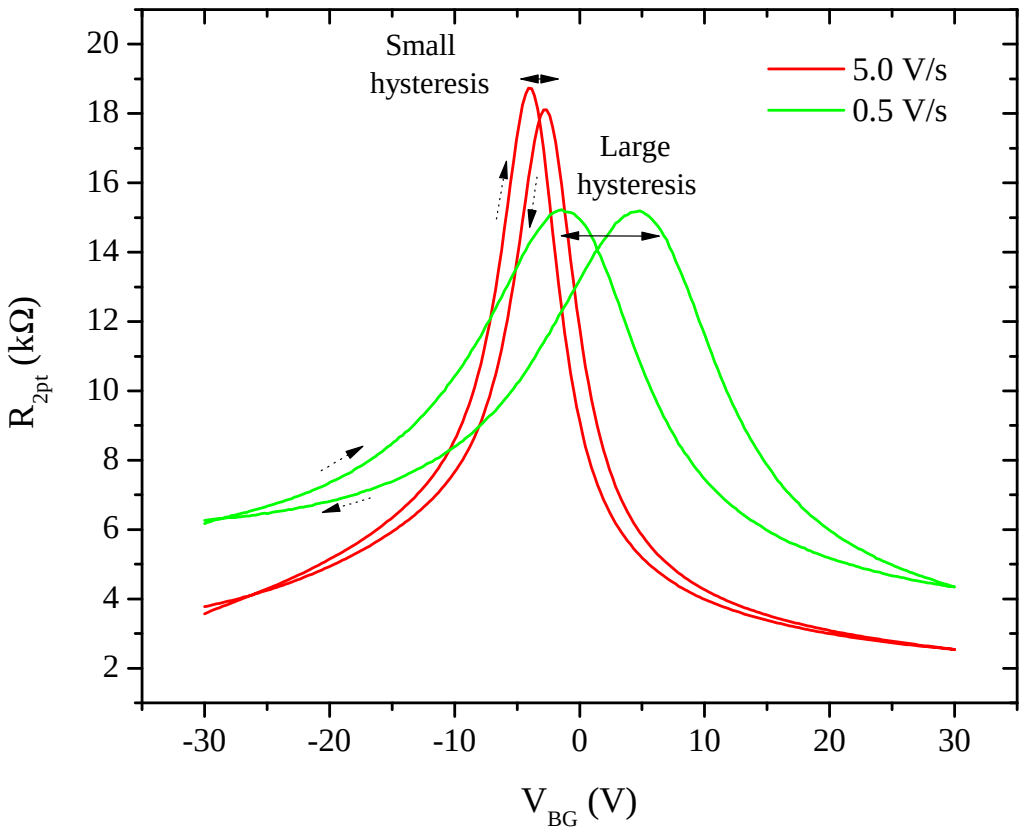


Figure 2.12: Hysteresis in GFETs at different back-gate voltage sweep rates

When the back-gate starts at a negative voltage, holes in graphene are slowly trapped into the trap centers, so that after some time the graphene sees a more positive potential than that simply due to the gate voltage (and vice versa for the opposite sweep direction) [39]. These trapped charges under graphene dope it and cause shifts in the Dirac point.

Charge traps seem to be charged on time scales comparable to the scale relevant for measurement [39]. To reduce this sweep dependent hysteresis, all measurements are made with the highest possible sweep rate to minimize charge trapping. Another way of reducing hysteresis in GFETs is by measuring them in a vacuum probe station which desorbs molecules from the surface of graphene.

2.4.3 GFETs using CVD graphene

As-fabricated back-gated GFETs made using Cu-grown CVD graphene are typically very highly p-doped due to PMMA and metal residues [40]. Figure 2.13 shows 4-point resistance of two different back-gated GFETs fabricated using Cu-grown CVD graphene. The carrier mobility is $\sim$ 1,300 cm^2/Vs and the Dirac voltage is around 40 V.

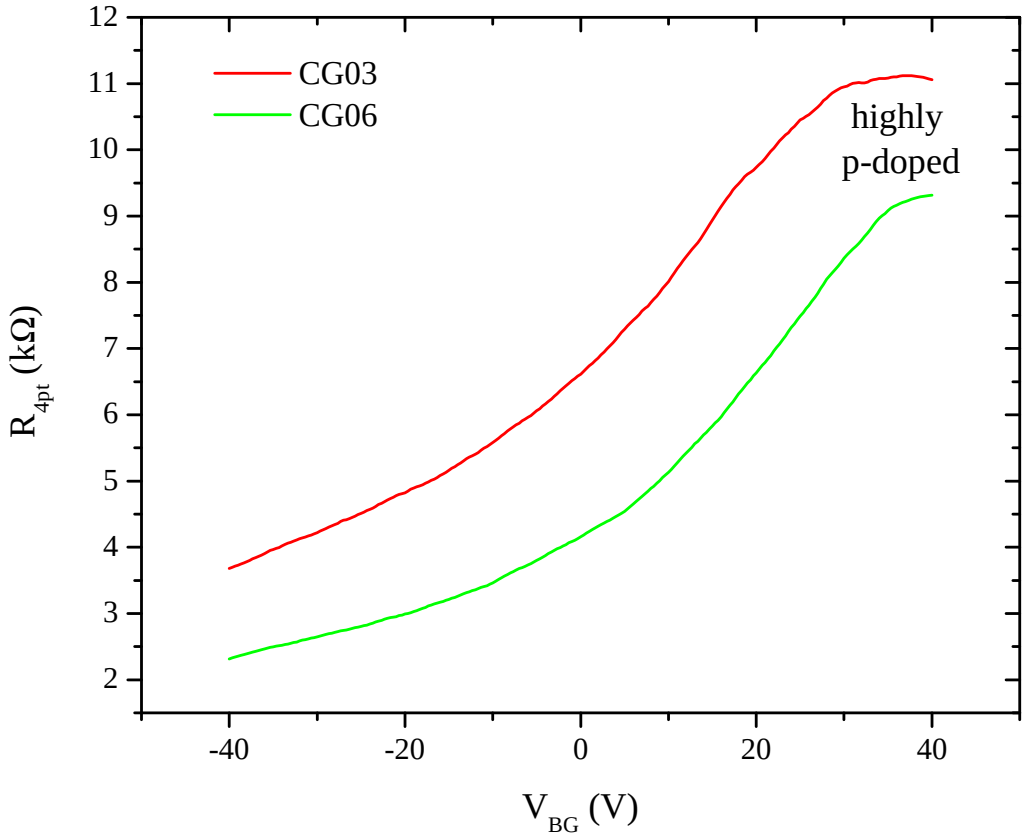


Figure 2.13: 4-point resistance of GFETs made with Cu-grown CVD graphene

Annealing the GFET in ultra-high vacuum gets rid of some of this p-doping and shifts the Dirac point closer to 0 V [40]. However, the vacuum level is very critical in order to not further damage the graphene. CVD graphene was hence avoided due to the need for extra processing and its low carrier mobilities.

2.4.4 Top-gated GFETs

Top-gated GFETs were fabricated using the process flow described in Figure 2.8 with 10 nm of ALD Al_2O_3 top-gate dielectric (on top of a 1.5 nm Al seed layer). Figure 2.14 shows the back-gated 2-point resistance measurements before and after depositing the top-gate stack.

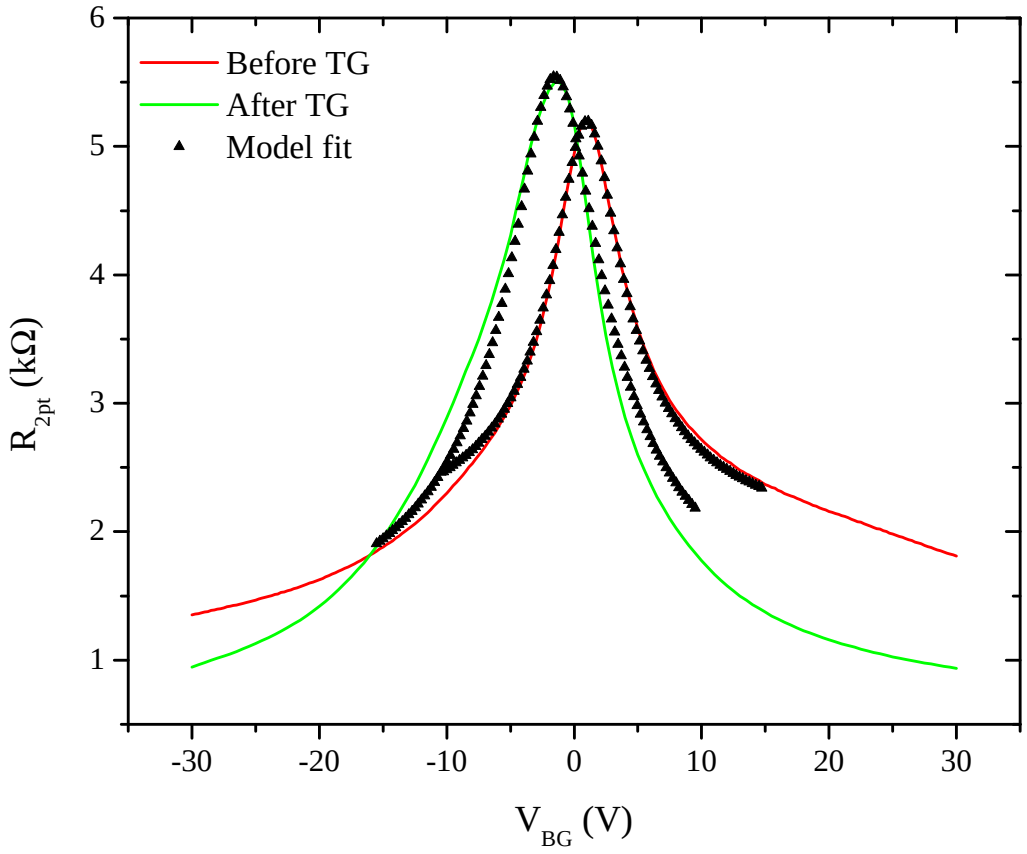


Figure 2.14: 2-point resistance of a GFET before and after top-gate stack deposition

Depositing the top-gate stack reduces the carrier mobility from 9,400 cm^2/Vs to 8,200 cm^2/Vs and dopes graphene slightly n-type (by -2.2 V). This could be due to fixed charges in the top-gate dielectric [41]. The model fit after top-gate deposition is also found to deviate significantly from the measured curve. This could be due to non-uniformities along the graphene channel leading to multiple regions with different

Dirac points and mobilities which skew the overall resistance curve.

This is more apparent in the top-gated 2-point resistance measurement shown in Figure 2.15 which shows a major Dirac point at $\sim$ -0.15 V and a minor Dirac point at $\sim$ -0.8 V.

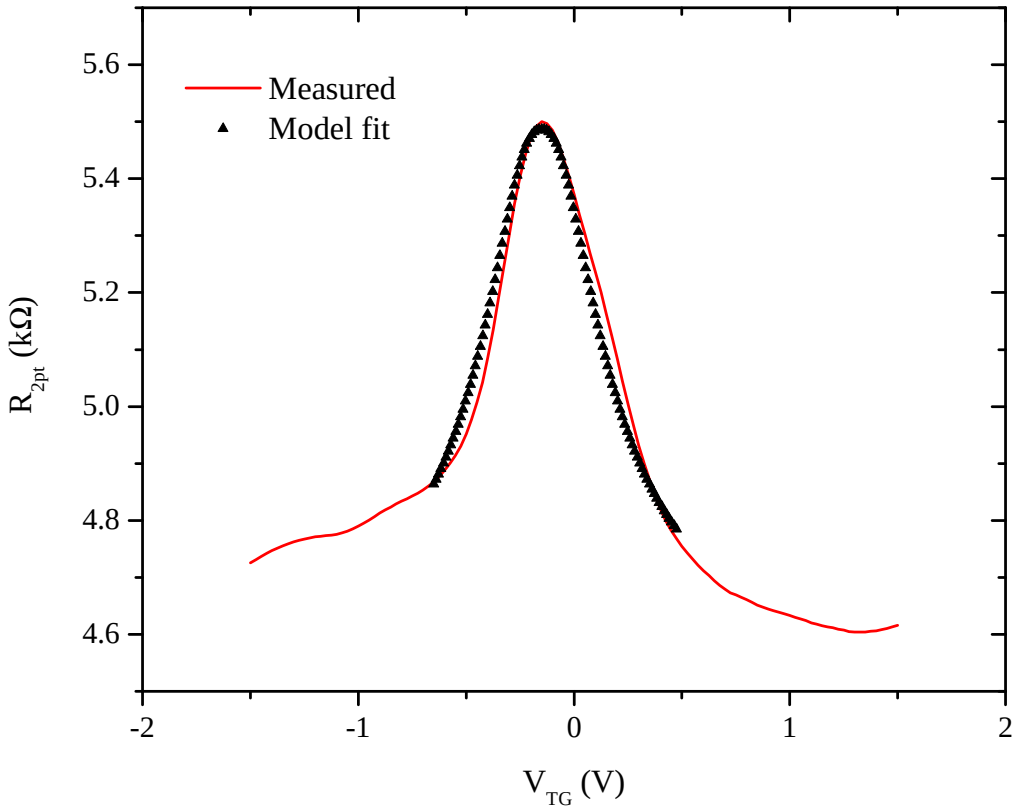


Figure 2.15: 2-point resistance vs. V_{TG} for a top-gated GFET

The model fit at low carrier concentrations gives a carrier mobility of 6,900 cm^2/Vs (W_G/L_G = 1.5μm/0.5μm for the top-gated region). The top-gate capacitance is backed-out from Figure 2.16 which shows the variation of the 2-point resistance of the GFET as a function of V_{BG} and V_{TG}.

A positive (negative) V_{BG} induces a finite concentration of electrons (holes) in the graphene channel, proportional to the back-gate capacitance (C_{BG}). Now, to restore the device to its Dirac point, a negative (positive) V_{TG} has to be applied to deplete

these excess electrons (holes) induced by V_{BG}. The V_{TG} required to deplete these excess electrons is related to V_{BG} by: $V_{TG} = C_{BG} \times V_{BG}/C_{TG}$ (which is just a way of writing the condition for charge neutrality at the Dirac point).

Marking the position of the Dirac point referred to the top-gate at every V_{BG} traces a line as shown in Figure 2.16. The slope of this line gives the ratio of C_{BG} to C_{TG} which is found to be $C_{BG}/C_{TG} = 0.024$. This gives a value of $C_{TG} = 462$ nF/cm^2. This corresponds to a dielectric constant of $\kappa_{Al_2O_3} \sim 5.5$ which is in accordance with reports from literature [42].

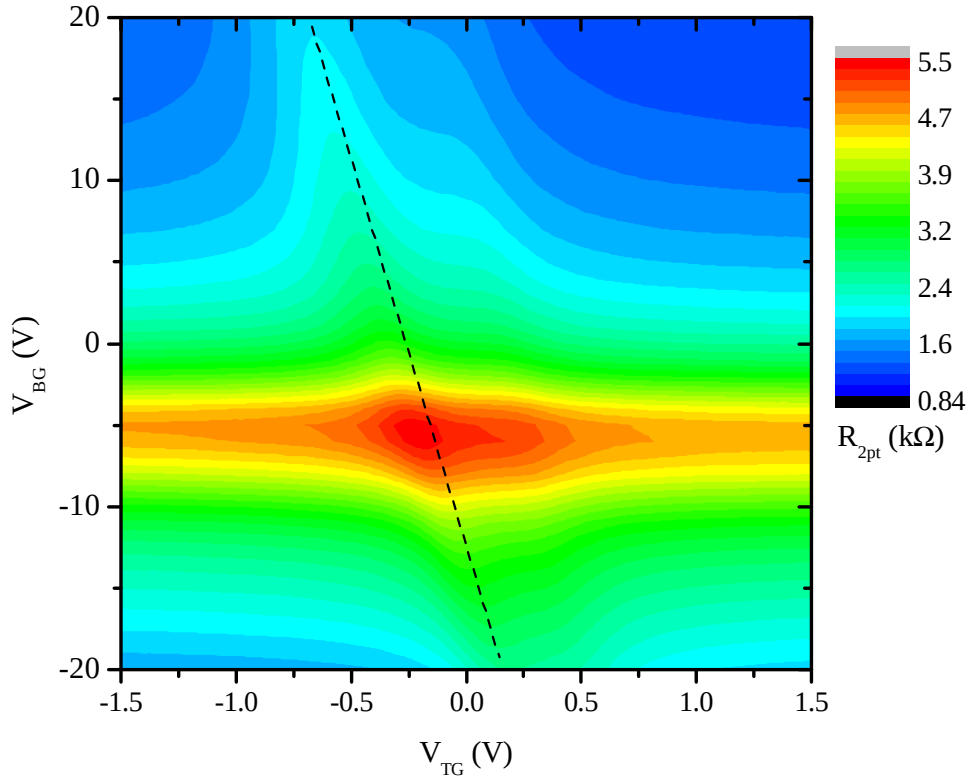


Figure 2.16: 2-point resistance of a top-gated GFET as a function of V_{BG} and V_{TG}

2.5 Summary

A review of literature reports of top-gated GFETs using various sources of graphene and various top-gate dielectrics was presnted. Methods of characterizing and identifying monolayer graphene for fabricating GFETs using optical microscopy, AFM and Raman spectroscopy were elaborated upon. A detailed fabrication flow for fabricating back-gated and top-gated GFETs was presented. Top-gated GFETs were fabricated using ALD grown Al_2O_3 seeded by a thin Al seed layer as the top-gate dielectric.

A model for GFET operation using a charge-sheet formulation with a Drude mobility scheme was presented. This model can be used to extract carrier mobilities and residual carrier concentrations from GFET electrical measurements. Back-gated GFETs fabricated on exfoliated monolayer graphene showed carrier mobilities up to 9,400 cm^2/Vs with a residual carrier concentration of $3\times10^{11}/cm^2$.

The effect of unintentional doping on the Dirac point of back-gated GFETs was studied. Doped GFETs typically end up having lower mobilities than their undoped counterparts. Hysteresis in the electrical characteristics of back-gated GFETs as a function of the back-gate voltage sweep rate was discussed. Back-gated GFETs were also fabricated using CVD grown graphene, but showed high p-type doping with low carrier mobilities of $\sim$ 1,300 cm^2/Vs.

Electrical measurements of top-gated GFETs showed slight n-type doping after depositing the top-gate dielectric along with a mobility degradation from 9,400 cm^2/Vs to 8,200 cm^2/Vs. The top-gated graphene region itself showed a mobility of 6,900 cm^2/Vs at low carrier concentrations. The top-gate capacitance was extracted by looking at dual-gated operation of the GFET, from the top-gate bias needed to neutralize excess carriers induced by a back-gate bias.

3

Doping of Graphene

Doping is the most feasible method of controlling the electronic properties of conventional semiconductors. Semiconductors can be doped n-type (with excess electrons) or p-type (with excess holes) by introducing impurities in them. These impurities (dopants) modulate the carrier concentrations either by accepting or donating excess electrons to the semiconductor. A similar approach can be used to dope graphene to make it n-type or p-type.

3.1 Doped graphene

A pristine graphene sheet free from impurities and disorder has its Fermi level at the Dirac point. In a back-gated GFET, this translates to the charge neutrality point (CNP) or Dirac voltage occurring at 0 V back-gate bias. But the inevitable presence of impurities typically shifts the position of the Fermi level away from the Dirac point leading to a CNP different from 0 V. However, a non-zero CNP is sometimes desired and can be achieved by intentionally doping the graphene.

Figure 3.1 shows a schematic of the bandstructures of (a) n-type doped graphene,

(b) intrinsic graphene and (c) p-type doped graphene. The shaded regions are occupied by electrons. The Fermi level (E_F) of n-type graphene lies above the Dirac point and the Fermi level of p-type graphene lies below the Dirac point in the bandstructure. Intrinsic graphene's Fermi level passes through the Dirac point.

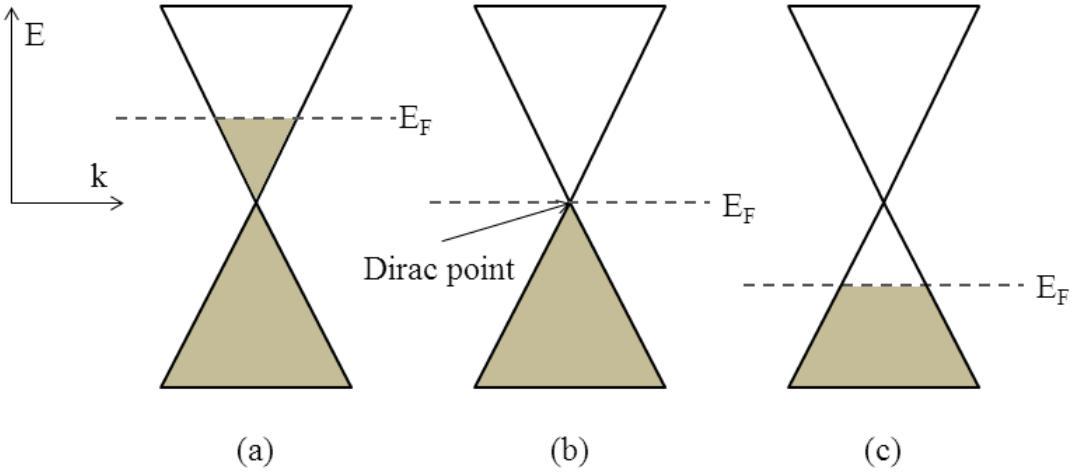


Figure 3.1: Schematic bandstructures of graphene.

A simple way of characterizing doping in graphene is by electrical measurements on back-gated GFETs [19]. The CNP of an intrinsic GFET lies at a back-gate bias (V_{BG}) of 0 V and the conductivity increases with both positive and negative V_{BG} to give the familiar Λ-shaped curve of resistance vs. V_{BG}. The CNP of p-type graphene however occurs at positive V_{BG} and the CNP of n-type graphene at negative V_{BG}. This is because, n-type (p-type) graphene needs to be biased at a negative (positive) V_{BG} in order to deplete excess electrons (holes) to move the Fermi level to the Dirac point.

Representative resistance vs. V_{BG} plots for intrinsic and doped GFETs are shown in Figure 3.2. The n-type and p-type GFETs are doped to -15 V and +15 V respectively. It is also assumed that doping does not effect mobility and residual impurity

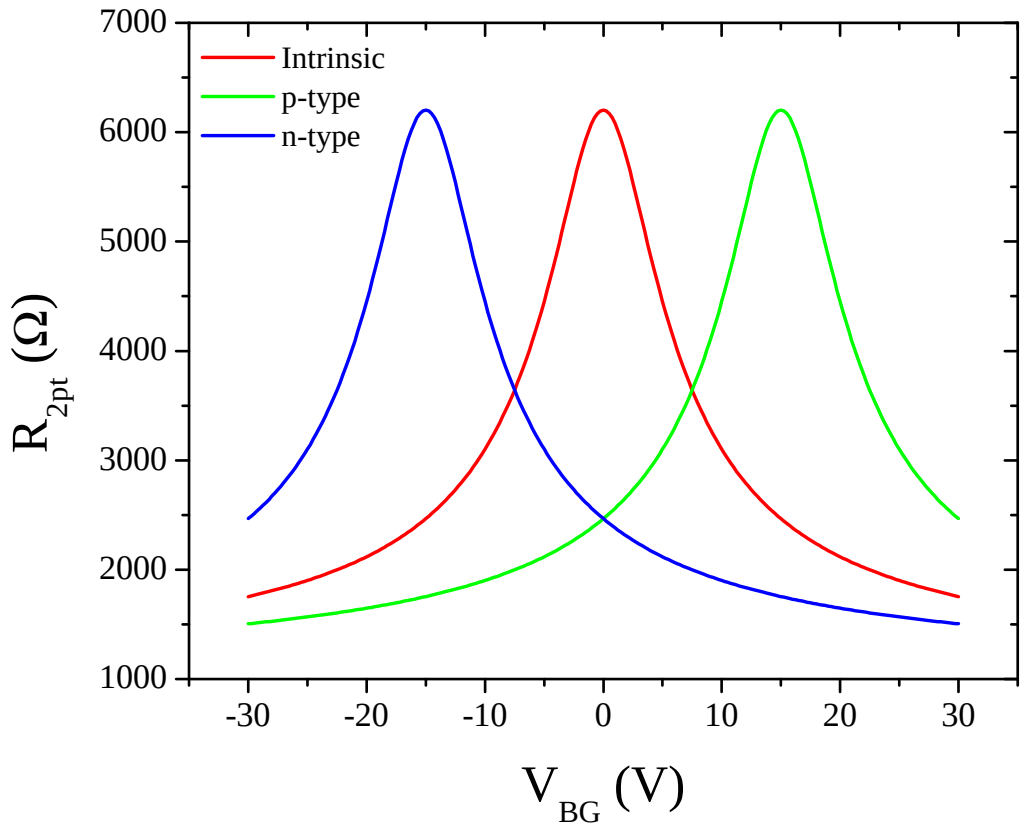
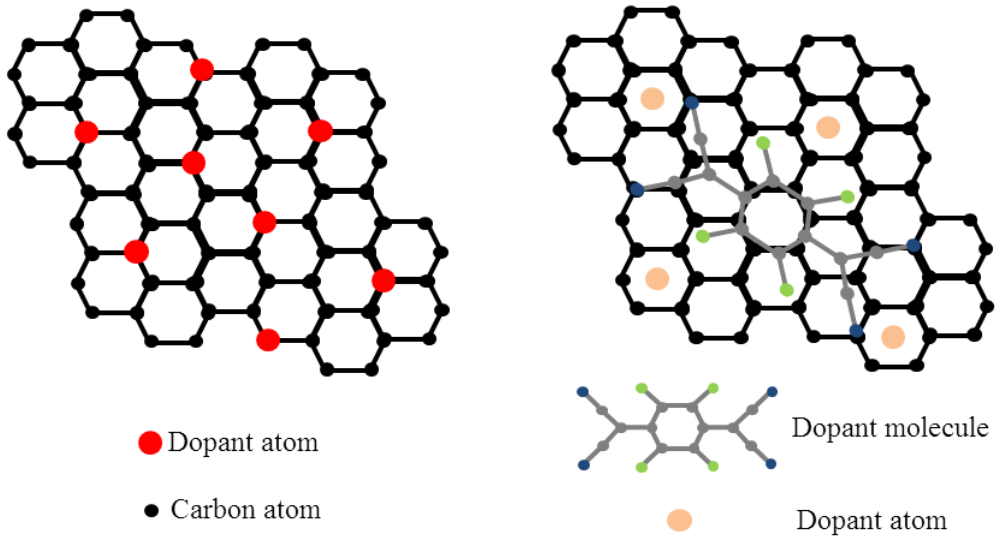


Figure 3.2: Resistance vs. V_{BG} for doped GFETs.

carrier concentration in this plot. This is evident from the shapes of the doped curves, which are mere displacements of the intrinsic curve to the CNPs of the doped cases. However, in reality, there is mobility degradation which shows up as a broadening of the resistance profile and a change in the residual carrier concentration which results in a resistance change at the CNP.

Doping in graphene can be broadly divided into two types: substitutional doping and surface transfer doping [18]. Substitutional doping refers to the substitution of a carbon atom in the graphene lattice with an atom having a different number of valence electrons such as nitrogen and boron. This is analogous to conventional doping in silicon. Surface transfer doping on the other hand is achieved by charge transfer between graphene and dopants which adsorb on the graphene surface. Figure 3.3

shows a schematic of (a) substitutional doping where dopant atoms (in red) substitute carbon atoms (in black) and (b) surface transfer doping where a dopant molecule or a dopant atom is adsorbed onto the graphene and dopes it.



(a) Substitutional Doping (b) Surface Transfer Doping

Figure 3.3: Schematic showing types of doping in graphene.

3.1.1 Characterization of doping

Doping in graphene can be characterized using three primary methods: photo emission spectroscopy (PES), especially X-ray photoelectron spectroscopy (XPS) and angle-resolved photoemission spectroscopy (ARPES), Raman spectroscopy and transport measurements [18].

Photoemission spectroscopy

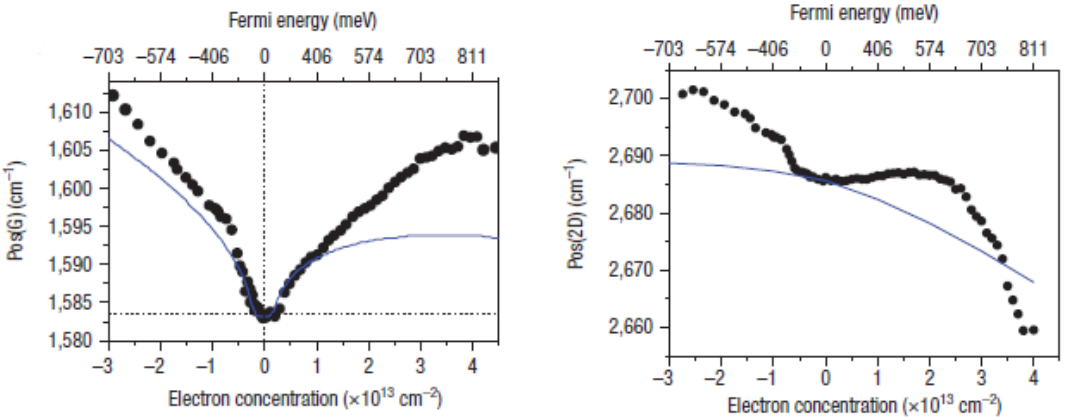
XPS measurements give the elemental composition of a material and it is possible to identify the dopant atoms in graphene using XPS. The doping level can be determined

by the relative intensity of the dopant peak with respect to the carbon peak. In case of substitutional doping, the chemical bonding and electric states of the dopants can also be obtained [43].

ARPES can be used to probe the electronic structure of graphene. The electronic bandstructure of graphene around the Dirac point can be measured along with the position of the Fermi level to get an estimate of the amount of doping [44].

Raman Spectroscopy

Raman spectroscopy is a powerful tool to measure the amount of doping in graphene, in addition to being able to monitor the number of layers and disorder. The G band stiffens and upshifts for both electron and hole electrostatic doping in graphene [45, 46] (Figure 3.4(a)). There is also a slight variation in the 2D peak position (Figure 3.4(b)). The positions of these two peaks can be used to quantify the amount of doping in graphene.



(a) Position of G peak

(b) Position of 2D peak

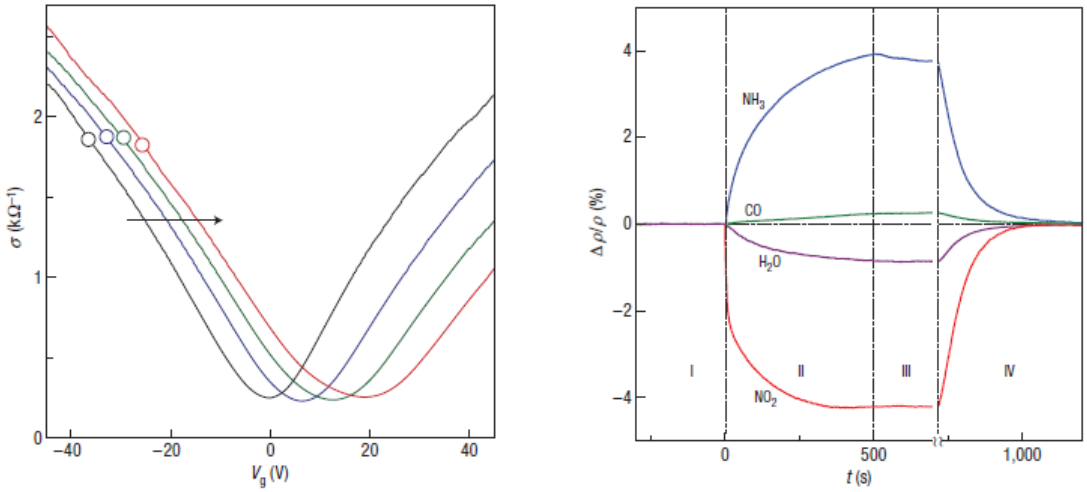
Figure 3.4: Raman peak positions with doping [46]

The Raman G peak is also sensitive to chemical doping. In chemically n-type doped graphene, the G band downshifts and stiffens and in p-type doped graphene, it

upshifts and softens [47]. The ratio of the 2D peak to the G peak (I_{2D}/I_G) is sensitive to both kinds of doping. In addition, there could be asymmetry or splitting of the G peak induced by surface transfer doping. Substitutional doping has a different effect on the Raman signatures, with both nitrogen and boron doped graphene showing an upshift of the G band [48].

Transport measurements

Electrical measurements done using field-effect devices on graphene give a direct indication of the amount and type (n-type or p-type) of doping. Figure 3.5(a) shows the evolution of the resistance profile of a GFET with increasing exposure to NO_2. The GFET is doped p-type by NO_2. The mobility of either electrons or holes is not affected by the dopant as evident from the steepness of the curves at different dopant concentrations [49].



(a) Evolution of resistance with exposure to NO_2

(b) Effect of various gases on resistivity

Figure 3.5: Effect of doping by gas adsorption on a back-gated GFET [49]

Figure 3.5(b) shows the changes in resistivity with exposure to various gases. Pos-

itive and negative signs are chosen to indicate electron and hole doping respectively. On annealing the graphene at 150 °C in vacuum, the dopants are desorbed and the initial undoped state is recovered [49].

3.1.2 Substitutional doping

Substitutional doping in graphene is primarily accomplished by replacing carbon atoms in the hexagonal honeycomb lattice by boron or nitrogen atoms. Theoretically, all Group III or Group V elements have the potential to substitutionally dope graphene, but boron and nitrogen are best suited for this because of their atomic sizes which are similar to carbon. Graphene with nitrogen atoms incorporated into the lattice dopes it n-type by donating electrons to the lattice and graphene doped with boron atoms dopes it p-type by accepting electrons from the lattice.

p-type doping

Table 3.1 summarizes literature reports of p-type doping using Boron.

Work	**Synthesis**	**Analysis**	**Notes**
L. Panchakarla *et. al.* [48]	Arc discharge in the presence of H_2 + B_2H_6	XPS + EELS + Raman	1.2 at. % of boron; sp^2 bonded boron; strong D-peak
T. Wu *et. al.* [50]	CVD on Cu using boric acid	XPS + Raman + Electrical	4.3 at. % of boron; sp^2/sp^3 bonded boron; $\sim$ 500 cm^2/Vs mobility
Z. H. Sheng *et. al.* [51]	Thermal annealing in presence of B_2O_3	XPS + Raman + TEM	Boron and oxygen doped; strong D-peak; presence of BC_2O species
L. Ci *et. al.* [52]	CVD of methane and ammonia-borane (NH_3-BH_3)	XPS + HRTEM + Raman + Electrical	h-BNC films; moderate D-peak; band-gap opening

Table 3.1: Reports of substitutional p-doped graphene from literature

Boron doping of graphene is typically done during growth by introducing precursors containing boron along with the carbon precursors. This type of doping induces a lot of defects in the graphene basal plane, as evident from the D-peaks. There is also very little control on the amount of doping [48].

n-type doping

Substitutional n-type doping in graphene is typically done by replacing carbon atoms with nitrogen atoms. Nitrogen atoms can be introduced into the graphene basal plane in "graphitic", "pyridinic" and "pyrolic" bonding configurations. Graphitic nitrogen refers to nitrogen replacing carbon with three sigma bonds. Pyridinic and pyrolic nitrogens on the other hand are bonded only to two carbon atoms, forming a hexagonal and a pentagonal ring respectively [53].

Work	**Synthesis**	**Analysis**	**Notes**
D. C. Wei *et. al.* [53]	CVD of methane (CH_4) and ammonia (NH_3)	XPS + EDX + Raman	8.9 at. % of nitrogen; sp^2/sp^3 bonded nitrogen; strong D-peak
X. Li *et. al.* [54]	Reduction of Graphene Oxide (GO) in NH_3	XPS + Raman + Electrical	5.0 at. % of nitrogen; sp^2/sp^3 bonded nitrogen; poor mobilities
Y. C. Lin *et. al.* [55]	Thermal annealing in presence of B_2O_3	XPS + Raman + Electrical	sp^2/sp^3 bonded nitrogen; strong D-peak; doping of $\sim 1\times10^{13}/cm^2$
Y. Zhen *et. al.* [56]	Chemical reduction of 4Cl-tetraPBIs	XPS + NMR	Primitive bottom-up approach of building GNRs; N-, O- doped

Table 3.2: Reports of substitutional n-doped graphene from literature

Attempts of substitutional n-doping in graphene are shown in Table 3.2. As with boron doping of graphene, nitrogen doping is also done during growth, where precursors containing nitrogen (typically NH_3) are introduced along with the carbon

sources. There have also been attempts to grow n-type doped graphene nanoribbons (GNRs) using a bottom-up approach by chemically reducing large aromatic molecules [56].

A common debilitating effect of substitutional doping is the generation of lattice disorder in the basal plane of graphene. This is because of size mismatch between the dopant atoms and carbon, which destroys the inherent hexagonal symmetry of graphene. This leads to degradation of carrier mobilities which is highly detrimental to GFET performance. Substitutional doping can however be used in certain cases to open bandgaps in graphene [52, 53, 55]. Tailoring the properties of graphene by substitutional doping is in its infancy and needs further investigation before it can be used as a viable method of doping.

3.1.3 Surface transfer doping

Surface transfer doping of graphene is accomplished by adsorbants on the graphene surface which are either electron-donating or electron-accepting. These adsorbants could be atoms or molecules and they do not generally disrupt the structure of graphene. Since adsorption is essentially a physical process, there is better control on the amount of doping and carrier mobilities do not degrade as much as in substitutional doping.

Charge transfer is determined by the relative position of density of states (DOS) of the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) of the dopant and the Fermi level of graphene. If the HOMO of the dopant species is above the Fermi level of graphene, electrons transfer from the dopant to graphene and dope it n-type. Similarly, if the LUMO of the dopant is below the Fermi level of graphene, electrons are transferred from graphene to the dopant,

thereby doping graphene p-type [18].

Generally speaking, molecules with electron withdrawing groups and electronegative atoms dope graphene p-type and molecules with electron donating groups and electropositive atoms dope graphene n-type. Since the adsorbants are only weakly bonded to the graphene basal plane, they can easily be desorbed and hence most cases of surface transfer doping are reversible [19].

p-type doping

The first GFET made on graphene was found to be p-type doped due to water vapor adsorbed on the graphene surface [5]. Unintentional doping like this affects most of the graphene devices when operating under ambient conditions.

Work	**Dopant species**	**Analysis**	**Notes**
F. Schedin *et. al.* [49]	Exposure to NO_2 gas	Electrical	Doping conc. $\sim 1.5\times10^{12}/cm^2$; negligible mobility degradation; desorption under vacuum
W. Chen *et. al.* [57]	Evaporation of F4-TCNQ[1]	PES	Bandgap opening of around 50mV
X. Dong *et. al.* [58]	Drop-casting with TPA[2] solution	Raman + Electrical	Doping of $\sim 8\times10^{12}/cm^2$; moderate D-peak and mobility degradation
N. Jung *et. al.* [59]	Intercalation by I_2 and Br_2	Raman	G-peak upshift and splitting; moderate D-peak; possible sp^3 bonded carbon
I. Gierz *et. al.* [60]	Evaporation of Bi, Sb and Au atoms	ARPES	Fermi level shifts by -0.8 eV; Linear dispersion of graphene is preserved

Table 3.3: Reports of p-doped graphene by surface transfer doping

[1] tetrafluoro-tetracyanoquinodimethane (F4-TCNQ) is a molecular electron acceptor

[2] tetrasodium 1,3,6,8-pyrenetetrasulfonic acid (TPA) has electron-withdrawing groups

Table 3.3 summarizes literature reports of p-type surface transfer doping using organic molecules and metal adatoms. Doping by organic molecules is typically done by evaporating the dopant species, where they get adsorbed onto the graphene or by dipping the graphene in a dopant solution [57, 58]. Metal adatom doping is done by evaporating a thin layer of the metal onto graphene under high vacuum [60].

n-type doping

Doping graphene n-type by surface transfer doping is achieved by selecting electron donating species as adsorbants.

Work	**Dopant species**	**Analysis**	**Notes**
F. Schedin *et. al.* [49]	Exposure to NH_3/CO gases	Electrical	Doping conc. $\sim 1.0\times10^{12}/cm^2$; negligible mobility degradation; desorption under vacuum
X. Dong *et. al.* [58]	Drop-casting with Na-NH_2[1] solution	Raman + Electrical	Doping of $\sim 3\times10^{13}/cm^2$;downshift of G peak; large mobility degradation
D. B. Farmer *et. al.* [61]	Soaking in a solution of PEI[2]	Raman + Electrical	Dopant-induced conductance asymmetry; hole mobility degrades after doping
J. H. Chen *et. al.* [62]	Exposure to potassium flux	Electrical	Overall mobility decreases; mobility asymmetry for holes vs. electrons increases
J. Choi *et. al.* [63]	Exposure to 4-amino-TEMPO[3]	STM + HRPES	Adsorption of radicals is seen in STM; downshift of Fermi level

Table 3.4: Reports of n-doped graphene by surface transfer doping

[1] 1,5-naphthalenediamine (Na-NH_2) is a molecular electron donor

[2] poly(ethylene imine) (PEI) is an electron donating macromolecule

[3] 4-amino-2,2,6,6-tetramethyl-1-piperridinyloxy (4-amino-TEMPO) is a free radical

A few attempts from literature of graphene surface transfer n-doping are shown in Table 3.4, where organic species like $NaNH_2$, PEI and 4-amino-TEMPO, gases like NH_3, CO and adatoms like potassium are used as dopants. As is the case with p-type doping, there is mobility degradation after n-doping.

Surface transfer doping is an easier method of doping compared to substitutional doping. There is also very little or no lattice disorder generated due to the dopants. The dopants only weakly interact with the π-orbitals of graphene and owing to this carrier mobilities are not adversely affected. There is also better control of the doping dose which is essentially proportional to the surface coverage of the dopant species. Surface transfer doping is also reversible, wherein the dopant species can be desorbed from the graphene surface.

Owing to its numerous advantages, surface transfer doping was chosen as the preferred method of doping in this work and attempts of doping graphene using different chemical species as adsorbants will be discussed in the next section.

3.2 Organic surface transfer doping

Surface transfer doping using organic molecules is a simple and straightforward method of doping graphene. By choosing molecules with electron accepting and electron donating groups, graphene can be doped p-type and n-type respectively. Experiments of doping graphene with various organic molecules and the methods used are presented in the following sections.

3.2.1 Doping using PMMA

PMMA (poly(methyl methacrylate)) is the primary EBL-resist used in GFET fabrication. As-fabricated GFETs typically have some PMMA residue on them, which

remains even after the acetone lift-off. This PMMA residue is partly responsible (along with adsorbed water vapor) for the unintentional p-type doping of as-fabricated GFETs [40]. This suggests that PMMA can also be used as an intentional dopant for doping graphene.

To test this hypothesis, electrical measurements were made on a back-gated GFET after spin-coating it with a solution of 4% PMMA (molecular weight 950,000) in chlorobenzene (PMMA C4) and opening windows over the contact pads using EBL. The standard spin-recipe of EBL-resist coating was used and the sample was baked at 180 °C for 2 minutes to drive away solvent residues. Figure 3.6 shows the 2-point resistance vs. V_{BG} of a back-gated GFET before and after spin-coating with PMMA.

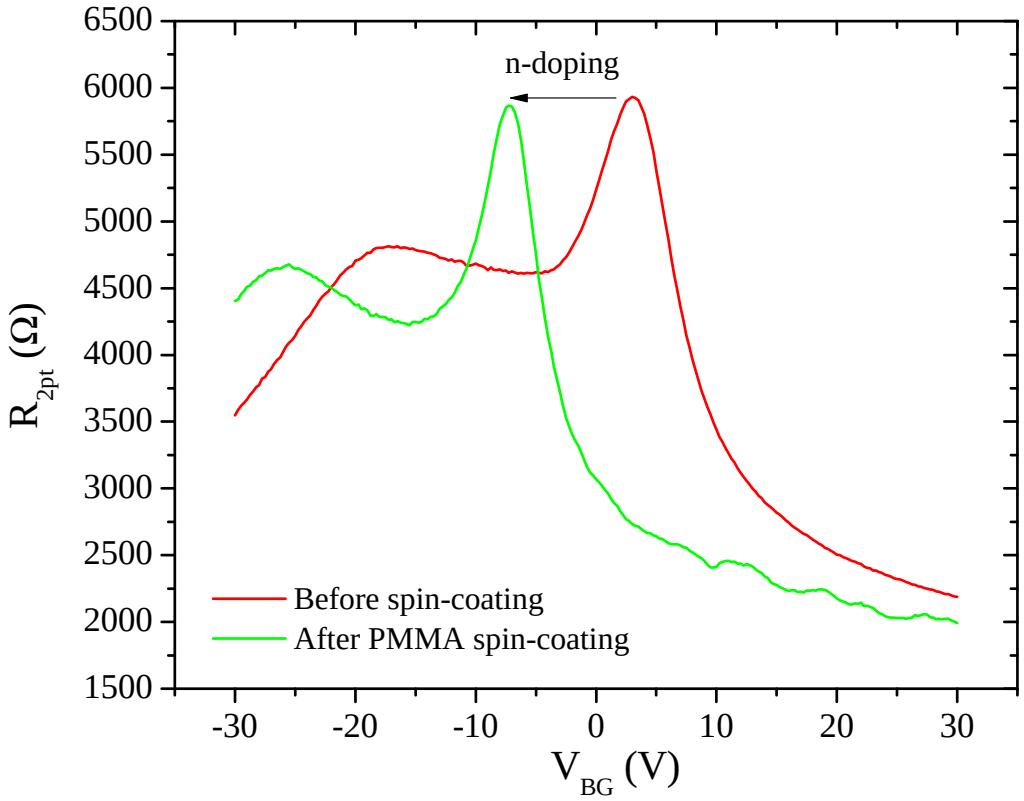


Figure 3.6: 2-point resistance vs. V_{BG} of a back-gated GFET before and after spin-coating with PMMA C4

The undoped resistance profile has two Dirac points: a primary Dirac point at 3 V and a secondary Dirac point at -17 V. This is because of two different regions of different unintentional doping levels on the graphene sheet, possibly due to impurities from device fabrication. However, after doping with PMMA, both these Dirac points shift by the same negative voltage, signifying n-doping. The shift in Dirac voltage is around -10 V, which corresponds to an n-doping concentration of $\sim 6.88\times10^{11}/\text{cm}^2$. Extraction of carrier mobilities for this device would not give accurate results because of multiple Dirac points. However, it can be seen from the slopes of the curves that there is no major mobility degradation after doping.

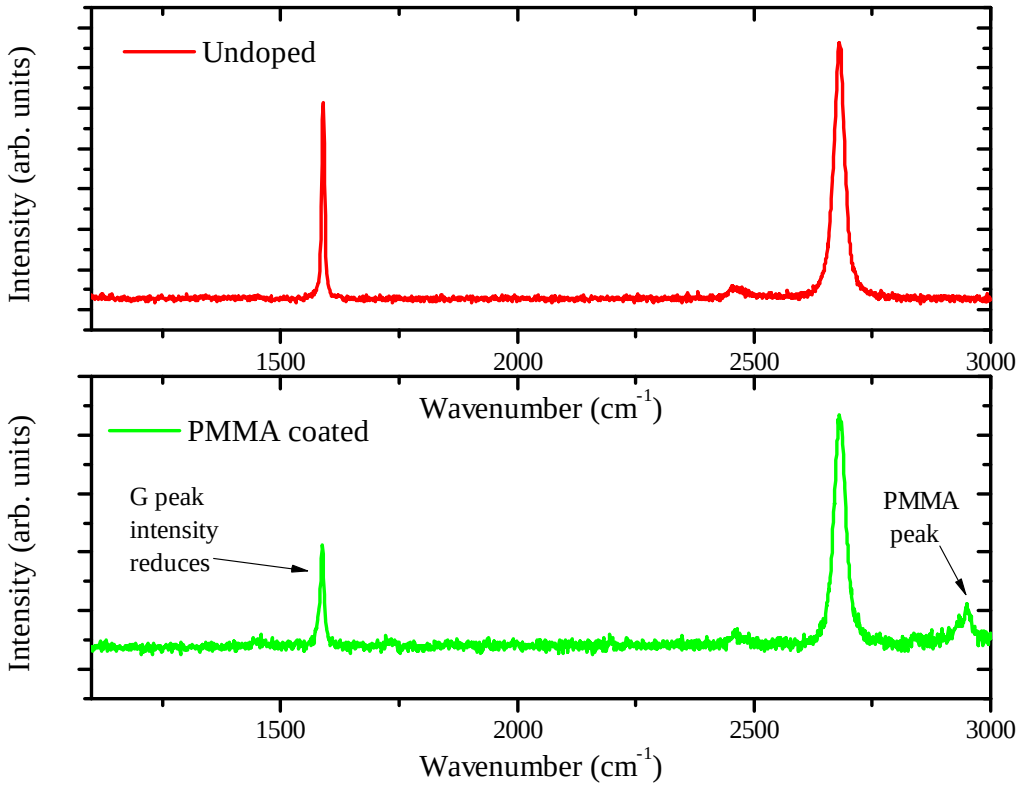


Figure 3.7: Raman spectra of graphene before and after spin-coating with PMMA C4

Raman spectra of graphene before and after spin-coating with PMMA are shown in Figure 3.7. A peak characteristic to PMMA appears at 2957 cm^{-1} which matches

with reports from literature [64]. There is also an increase in the 2D to G peak intensity (I_{2D}/I_G) from 1.3 to 2.2 signifying doping. PMMA does not cause any lattice defects in graphene which is evident from the absence of a D peak.

While A. Pirkle *et. al.* [40] show PMMA residue to cause p-type doping in graphene, the results presented here convey n-type doping action of PMMA. This discrepancy is possibly because PMMA residues vary in chemical composition and/or bonding to the graphene lattice when compared to pure spin-coated PMMA. The very existence of PMMA residues implies that they are not like pure PMMA, but are possible chemical modifications that are differently bonded to graphene. If they were actually just like pure PMMA, they would have been washed away during acetone lift-off.

These results suggest that PMMA can be used as an n-type surface transfer dopant. The doping concentration can be controlled by changing the concentration of the PMMA solution and the spin-coating speed.

3.2.2 Doping using TCNQ

Tetracyanoquinodimethane (TCNQ) is a powerful electron acceptor and is expected to dope graphene p-type [65]. Flourinated derivatives of TCNQ like F4-TCNQ have also been previously reported to dope graphene p-type [57]. One way of doping is by thermal evaporation of TCNQ onto graphene under high vacuum. An easier method is liquid-phase doping, where a solution of TCNQ in an appropriate solvent is used to transfer the dopant onto graphene.

TCNQ has a high solubility in N,N-Dimethylformamide (DMF), which is a well-known organic solvent. To dope graphene, a dilute solution of 0.2% wt. TCNQ in DMF was prepared by magnetic stirring in a dark container for 2 days. The solution

changed color from yellow-green to deep-blue after 6 hours. No further change in color was observed. A clean back-gated GFET was immersed in this solution for 30 minutes to let the dopant adsorb onto the graphene surface and was subsequently baked on a hot plate at 180 °C for 2 minutes to drive away solvent residues.

Figure 3.8 shows a plot of the 4-point resistance of the back-gated GFET before and after doping with the TCNQ solution. There is a large positive shift of the Dirac voltage ($+ \sim 100V$), which corresponds to a p-doping concentration of $\sim 6.88\times10^{12}/\text{cm}^2$. There is also a large degradation in carrier mobilities which is apparent from the broadening of the resistance profile around the Dirac voltage.

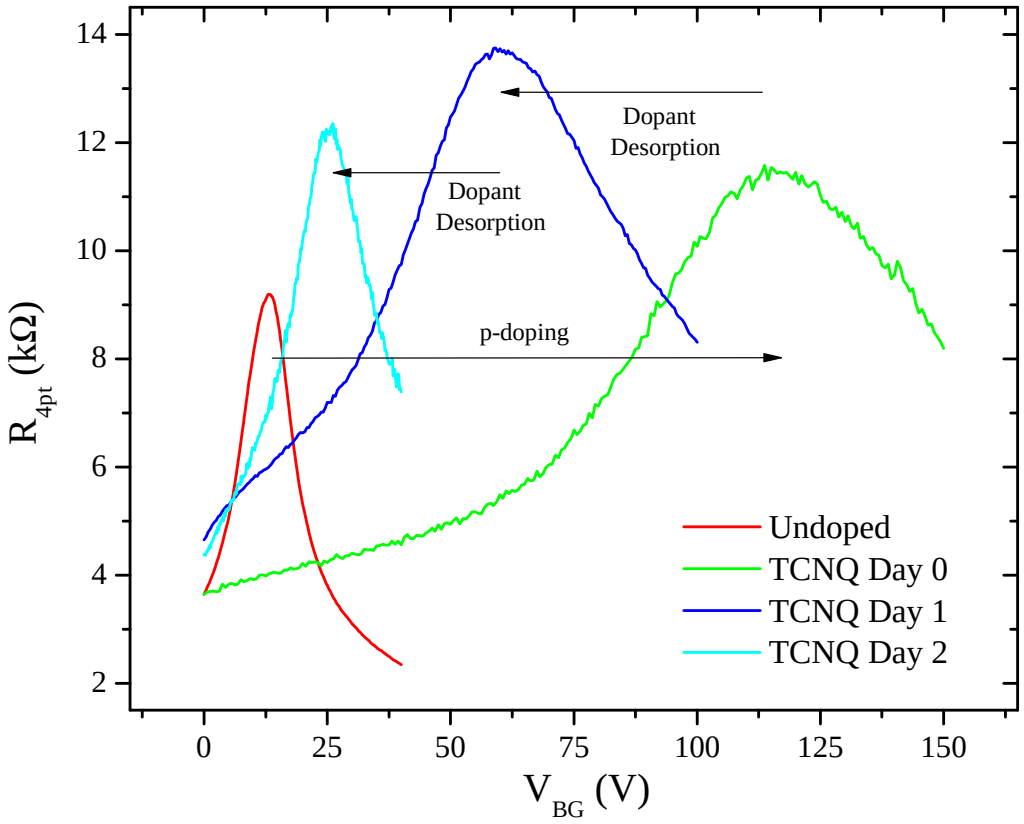


Figure 3.8: 4-point resistance vs. V_{BG} of a back-gated GFET before and immediately after doping with TCNQ, after 1 day and 2 days in ambient

The GFET was left under ambient conditions and electrical measurements were

made in intervals of 24 hours to check if there was desorption of the TCNQ. Figure 3.8 shows the resistance profiles of the back-gated GFET after leaving it under ambient conditions for a period of 1 and 2 days. The Dirac point moves to lower voltages signifying desorption of the dopants. There is also an increase in carrier mobilities, which is evident from sharpening of the resistance profile around the Dirac voltage with time.

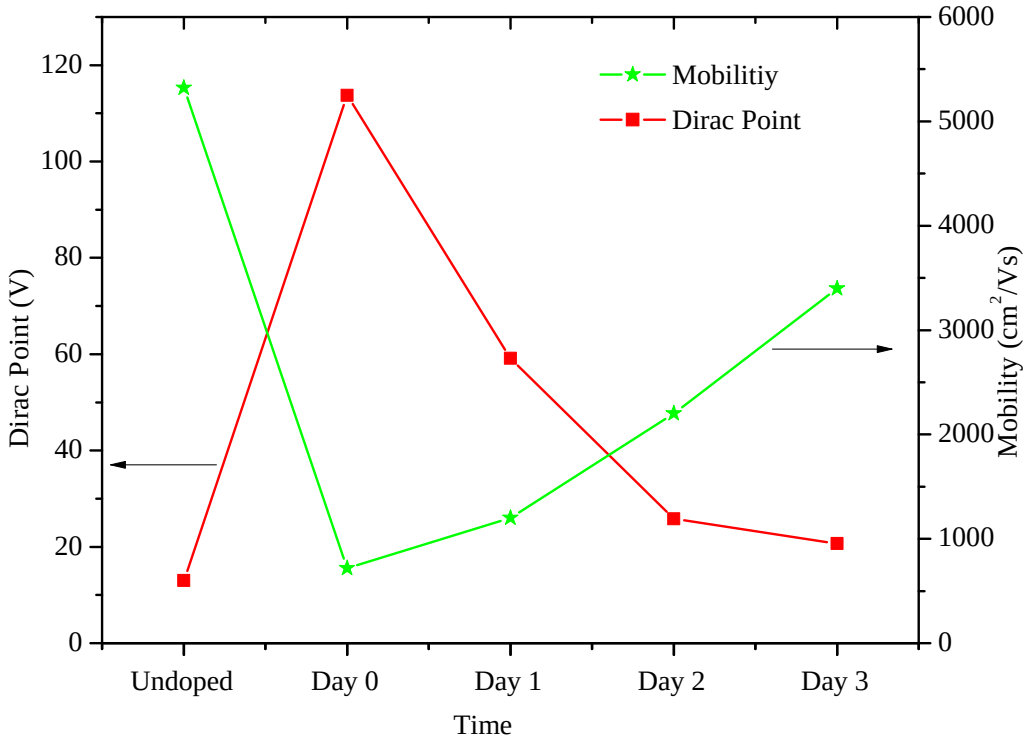


Figure 3.9: Change in position of the Dirac point and extracted carrier mobility of the GFET due to dopant desorption over time

Figure 3.9 shows a plot of the change in the position of the Dirac point and the change of carrier mobilities over time due to dopant desorption. The Dirac point moves closer to the undoped value and the carrier mobility improves with dopant desorption. However, there is some dopant which does not desorb from the surface and causes permanent p-type doping of the graphene (by +7 V). The final carrier

mobility stabilizes at 4200 cm^2/Vs, which is less than the undoped mobility of 5300 cm^2/Vs. This is expected due to additional scattering from the dopant species.

3.2.3 Doping using PEI

PEI (poly(ethylene imine)) is a polymer with amine-rich, electron-donating groups and has been used as an n-type dopant on carbon nanotubes. PEI can also be used to dope graphene n-type [61]. The same approach used for TCNQ doping can be extended for PEI doping.

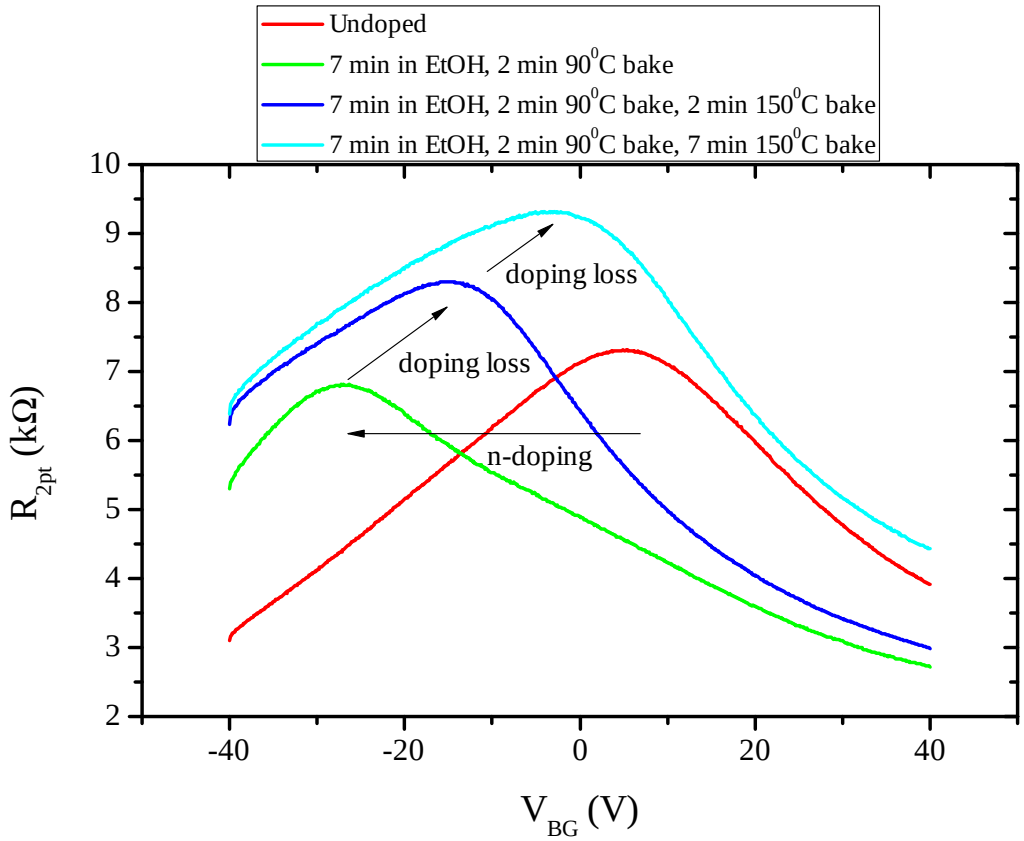


Figure 3.10: 2-point resistance measurements on a back-gated GFET after doping with PEI, courtesy of Michael Ramon

Figure 3.10 shows 2-point resistance measurements on a back-gated GFET doped using a 0.1% solution of PEI in methanol. The GFET was immersed in the dopant

solution for 30 minutes to let the dopant molecules adsorb onto the graphene surface. Electrical measurements after this step showed very large n-type doping with the Dirac point outside the voltage range accessible by the back-gate. It was observed that leaving the GFET under ambient conditions did not desorb the PEI molecules like in the case of TCNQ. This is probably because of the large molecular weight of PEI which makes it hard to desorb.

The GFET was then cleaned in ethyl alcohol (EtOH) to remove some of the PEI and baked on a hot-plate at 90°C for 2 minutes. The doping level was found to reduce due to desorption of the dopant. The Dirac voltage shifted by - 35 V with respect to the undoped one after this step, corresponding to an electron doping concentration of $\sim 2.40\times10^{12}/\text{cm}^2$. There was no difference in the residual impurity concentration.

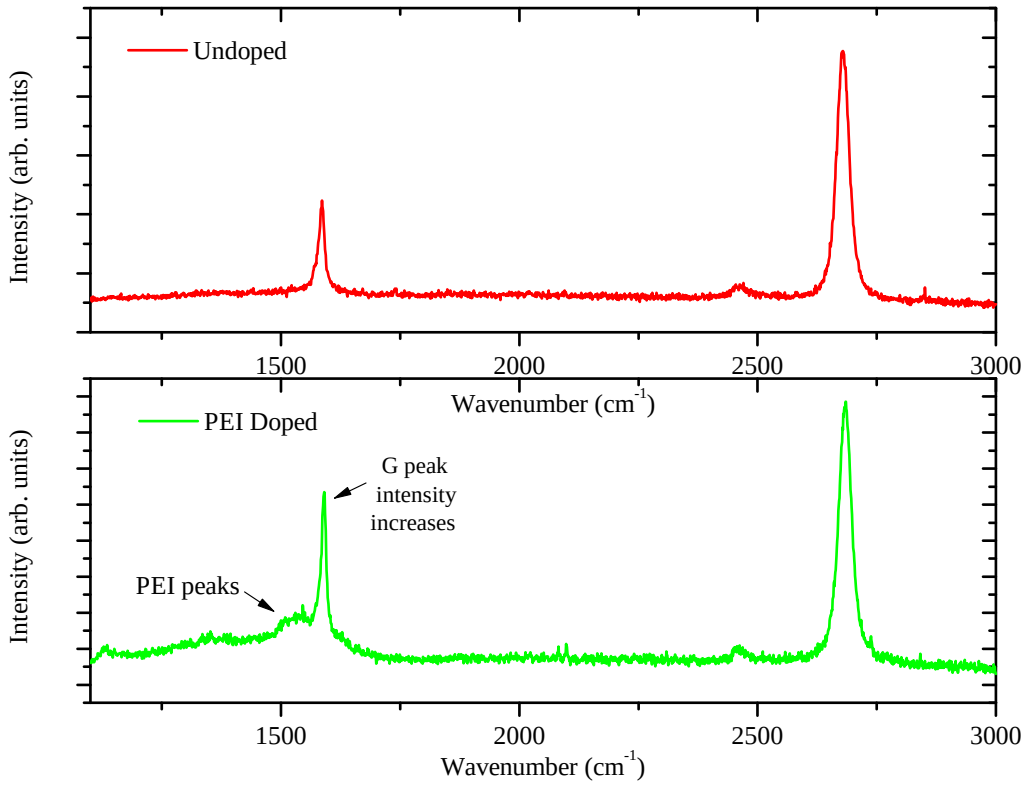


Figure 3.11: Raman spectra of graphene before and after doping with PEI

To further de-dope the dopant molecules, the GFET was baked at 150°C for 2 minutes and 7 minutes and electrical measurements were taken after each baking step (Figure 3.10). The amount of doping was found to reduce after both the baking steps which is due to desorption of the dopant.

Figure 3.11 shows the Raman spectra of graphene before and after doping with PEI. The 2D to G peak intensity reduces after doping and peaks characteristic to PEI appear around 1500 cm^{-1} and 1050 cm^{-1}. There is no D peak which signifies absence of disorder in the graphene plane after doping.

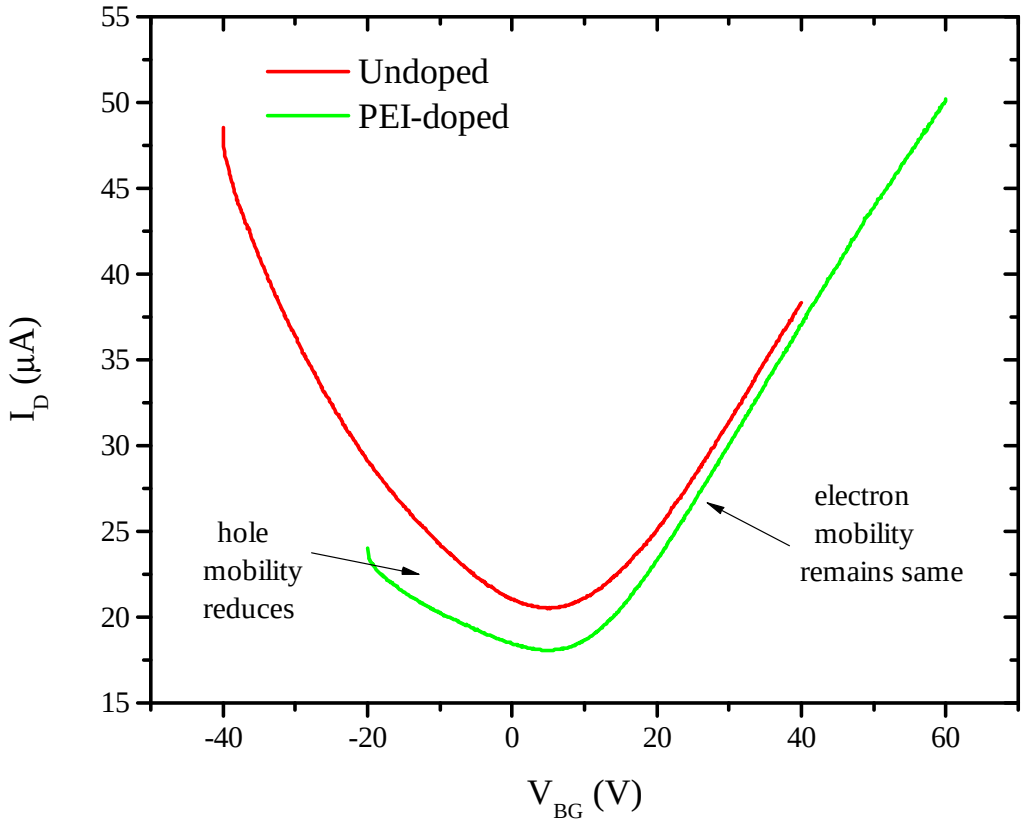


Figure 3.12: Dirac point normalized I-Vs showing conduction asymmetry after PEI doping

Normalizing the I_D-V_{BG} plots before and after doping with respect to the Dirac point shows a conduction asymmetry between electrons and holes as shown in Fig-

ure 3.12. The hole conductance is suppressed and the electron conductance is preserved. The hole mobility reduces from 2,000 cm^2/Vs to 1,600 cm^2/Vs and the electron mobility remains at 2,000 cm^2/Vs after doping. This is in accordance with reports from literature [61].

Immersing graphene in dopant solutions offers very little control on the amount of doping. The dopant adsorption is essentially self-limited and in most cases the graphene gets degenerately doped to a large Dirac voltage. An alternate way is to use the idea of spin-on-doping.

Spin-on-doping of PEI

Instead of immersing graphene in the dopant solution, the dopant can be spin-coated onto the graphene surface. This method offers better control on the doping dose. The concentration of the dopant solution would now be a direct knob to control the doping dose. By choosing a sufficiently low concentration, moderate doping levels can be attained.

A dilute solution (0.02 % by wt.) of PEI in methanol was prepared by magnetic-stirring in a dark container for 2 days. This solution was then spin-coated onto a back-gated GFET until the solvent evaporated. A spin speed of 1500 rpm and a spin time of 1 minute was chosen. The sample was then baked at 90°C for a minute to evaporate any residual methanol from the graphene surface. Figure 3.13 shows the 4-point resistance measurements of the GFET before and after doping.

Control of the amount of doping can be achieved by repetitively spin coating the GFET with the dopant solution. Figure 3.13 shows the effect of a second spin-coating step on the Dirac voltage. The Dirac voltage moves further to a more negative voltage signifying increasing n-doping.

The conduction asymmetry observed between electron and hole conduction is also

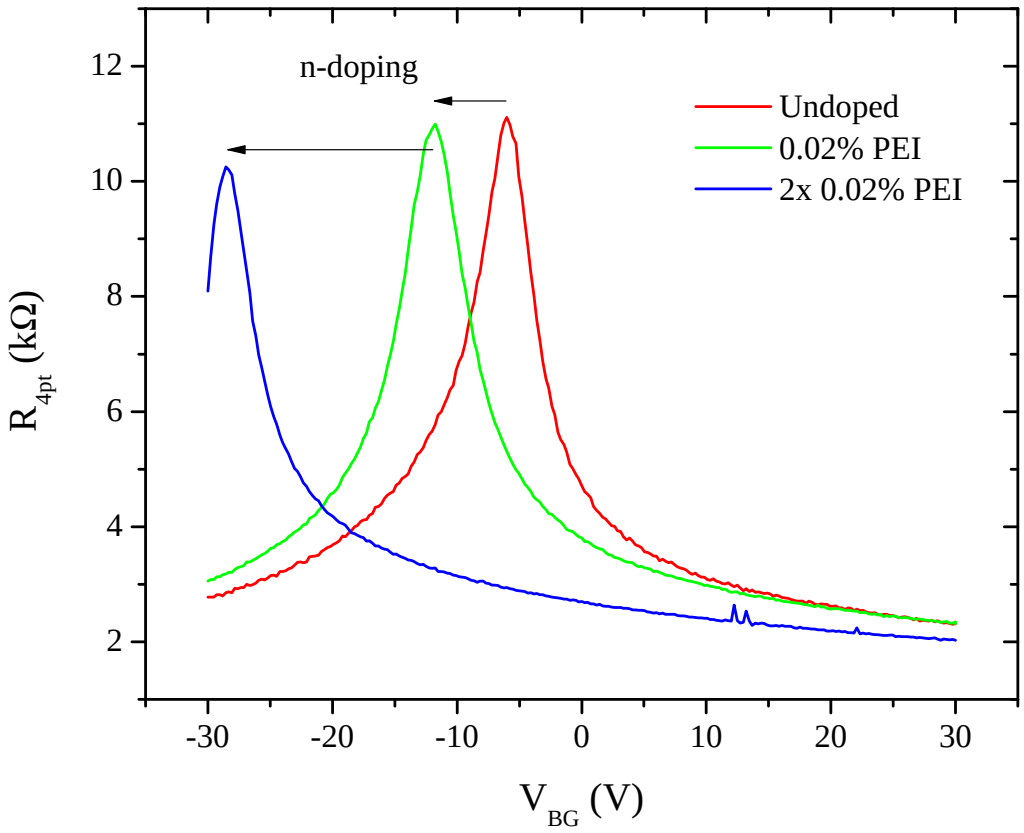


Figure 3.13: 4-point resistance measurements on a back-gated GFET doped with PEI

seen after spin-doping. Hole conduction is suppressed and electron conduction is preserved.

PEI was chosen as the preferred dopant for self-aligned doping of the access regions of top-gated GFETs because of its ease of application. A detailed analysis of spin-on-doping on the mobilities and the amount of doping is presented in Chapter 4.

3.3 Doping loss

Surface transfer dopants are weakly bonded to the graphene basal plane [18]. These dopants can easily be removed by cleaning the sample in a solvent that dissolves the dopant or by annealing the graphene. The dopants also get desorbed from the

graphene surface even when it is just exposed to ambient conditions [66].

Figure 3.8 shows the effect of TCNQ desorption (doping loss) when the GFET is exposed to ambient conditions. There is desorption of the dopant until it reaches a natural equilibrium and does not de-dope any further. Figure 3.10 shows doping loss by annealing when ambient doping loss is not possible or very slow. Doping loss by annealing is much quicker than doping loss under ambient conditions.

While doping loss is undesired, it can be used to control the amount of doping. Annealing could cause the dopants to react with graphene and change its properties, but doping loss under ambient conditions or under vacuum is a simple way of reducing the amount of doping.

3.3.1 Doping loss in vacuum

When a doped GFET is pumped down under vacuum, there is desorption of the dopant species from the graphene surface. This is essentially due to diffusion of the dopant away from the graphene driven by a concentration gradient.

Figure 3.14 shows the evolution of the I-V of a back-gated GFET after pumping in vacuum over a period of 6 days. The GFET was doped unintentionally to around + 3 V after device fabrication. This could be because of PMMA residues or adsorbed water vapor.

The Dirac voltage was found to move closer to 0 V on pumping down in vacuum. There was rapid desorption to start off which stabilized with time. The Dirac voltage stopped moving after around 6 days in vacuum. On exposing the graphene to ambient, there was a slight shift of the Dirac voltage, but to a negative value (-2 V). Resistance at the Dirac point increased with time under vacuum which signified reducing residual impurity concentration.

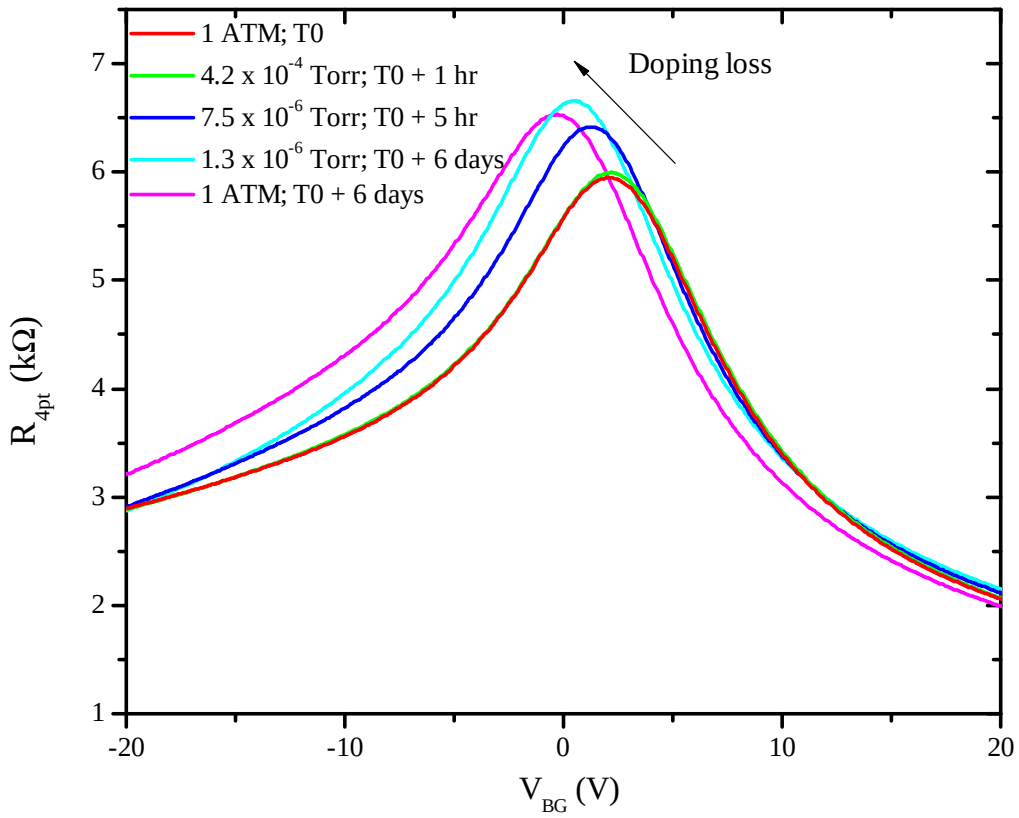


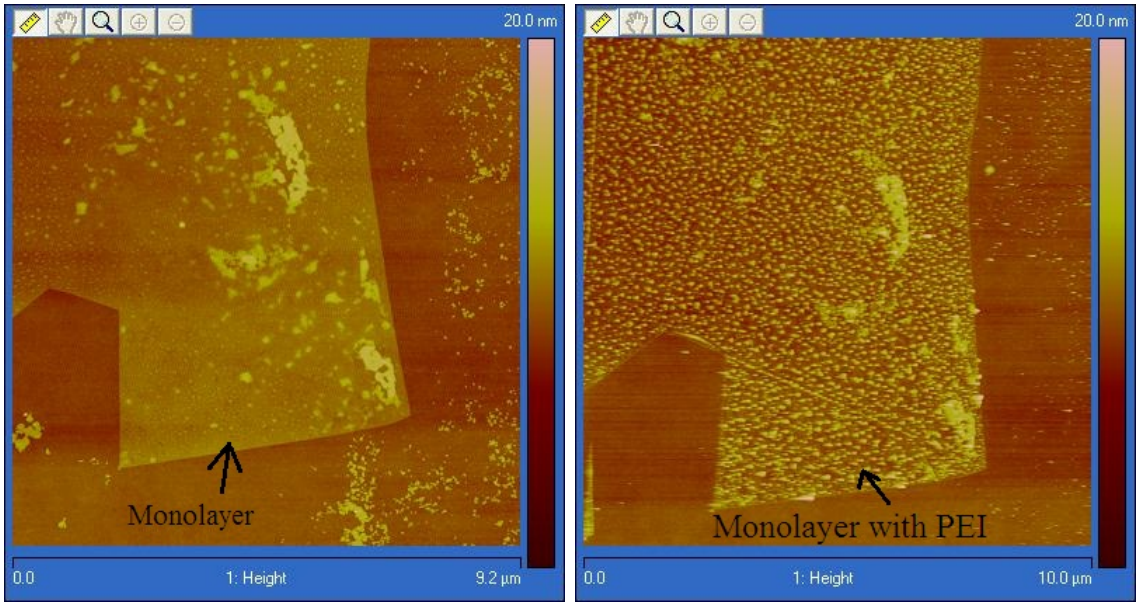
Figure 3.14: 2-point resistance measurements of loss of doping in a GFET under vacuum, courtesy of Michael Ramon

3.3.2 Capping by ALD

Desorption of dopants under ambient conditions causes a drift in the position of the Dirac voltage. This can be prevented by sealing the dopants on graphene with a capping layer. This would prevent desorption of the dopant species and result in stable device characteristics over time.

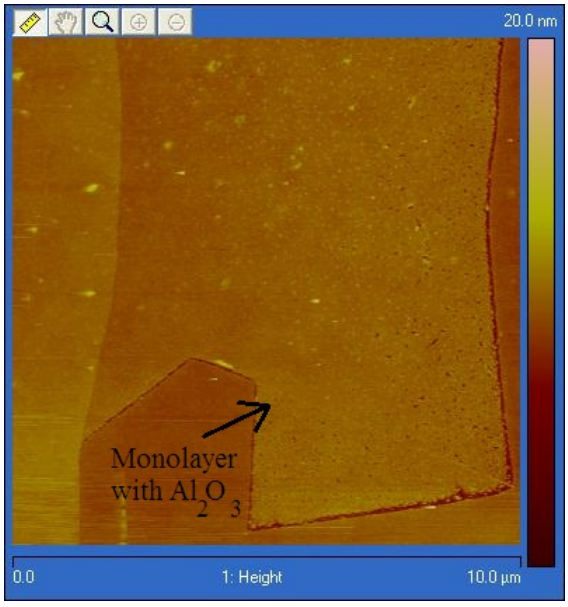
PEI is a hydrophilic molecule and can be used as a seed layer for ALD growth of Al_2O_3 [67]. There is no need to use a separate Al seed layer. If the ALD growth is started with the water cycle, H_2O molecules attach to the PEI dopants on graphene and the subsequent cycles can continue. Figure 3.15 shows AFM scans of a monolayer flake before, after doping and after depositing a 10 nm ALD Al_2O_3 capping layer.

It can be seen from Figure 3.15(b) that the PEI agglomerates as small clusters on the graphene surface. These clusters act as seeds for ALD growth. The graphene surface is as smooth as pristine graphene after the ALD deposition.



(a) Before doping

(b) After doping with PEI



(c) After capping with ALD Al_2O_3

Figure 3.15: AFM images of graphene before and after doping and ALD capping

A 10 nm Al_2O_3 layer is sufficient to cap the dopants intact and prevent desorption [67]. Further processing can now be done on this capped graphene, say, if it is to be used in an integrated circuit. Capped GFETs can also be used in ambient conditions without any concerns of dopant desorption.

3.4 Summary

Doping graphene changes the position of its Fermi level relative to the Dirac point. Intrinsic graphene has its Fermi level passing through the Dirac point, n-doped graphene has its Fermi level above the Dirac point and p-doped graphene below the Dirac point. This translates to n-doped GFETs having a negative Dirac voltage, intrinsic GFETs having a zero Dirac voltage and p-doped GFETs having a positive Dirac voltage.

Doped graphene can be characterized using photoemission spectroscopy, Raman spectroscopy and electrical transport measurements. Doping in graphene can be broadly classified into two types: (1) substitutional doping where a dopant atom substitutes a carbon atom in the graphene lattice and (2) surface transfer doping where a dopant species is adsorbed on the graphene plane and dopes it. Various literature reports of doping graphene using these methods was presented.

Surface transfer doping is a relatively simpler method of doping graphene compared to substitutional doping. The effects of various surface transfer dopants like PMMA, TCNQ and PEI were studied in detail. Spin-on-doping of PEI was discussed and was found to have very little effect on the mobility of graphene. PEI could also be applied onto graphene using a simple spin-on-doping approach. PEI was hence chosen as the preferred dopant for doping the access regions of top-gated GFETs.

Desorption of dopants from graphene was studied under vacuum. An ALD-capping scheme was developed to seal the dopants and prevent doping loss.

4

Self aligned GFETs with surface transfer doped source/drain access regions

The exceptional electronic properties of graphene make graphene field effect transistors (GFETs) promising candidates for post-CMOS devices. In particular, the high intrinsic carrier mobility of graphene (greater than 10,000 cm^2/Vs at room temperature) and a large saturation velocity ($\sim 5.5\times10^7$ cm/s) exceed the corresponding values of silicon [68]. In this chapter, a novel scheme of fabricating GFETs with self-aligned spin-on-doped source/drain access regions is described. An improvement of up to $\sim$ 4X in GFET drive currents is reported.

4.1 Self-aligned GFETs

A major factor responsible for degradation of GFET performance is the series resistance of the access regions between the source/drain electrodes and the top-gated

graphene channel. GFET drive currents are adversely affected due to this series resistance and optimal transistor performance is impeded. This problem had plagued conventional Si CMOS transistors in the past and was overcome by using a self-aligned gate fabrication approach [69].

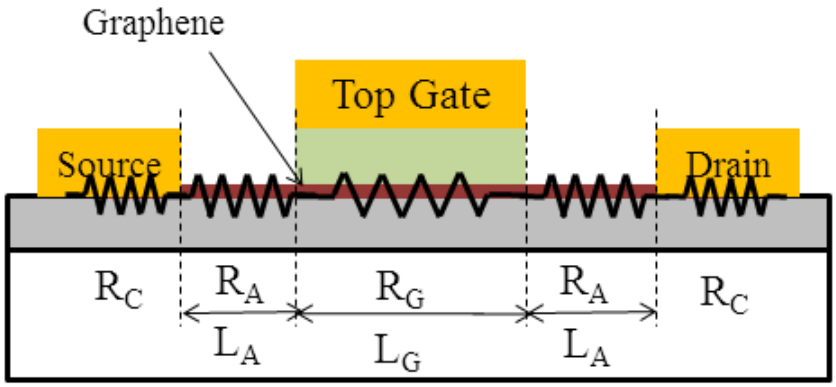


Figure 4.1: Schematic of a GFET showing various resistance contributions

Figure 4.1 shows the schematic cross-section of a top-gated GFET. The resistance of the top-gated graphene region is denoted by R_G, the contact resistance between the source/drain electrodes and the graphene is denoted by R_C and the access region resistance is denoted by R_A. Reduction of R_A and R_C can substantially improve analog and radio frequency (RF) performance metrics such as transconductance, transit frequency and self-gain [70].

An obvious way of reducing the access resistance is by using the back-gate as a knob to electrostatically induce carriers [34]. While this approach does reduce the access resistance, it cannot be used in the case where there are multiple transistors on the same substrate. A back-gate bias would equally effect all transistors on the substrate; independent control of each transistor would not be possible. Also, this approach fails when the substrate is insulating (which is preferred for RF transistors,

to reduce parasitic capacitances).

While the contact resistance R_C is determined by the choice of metal and the graphene to metal contact area, the access region resistance R_A is primarily dependent on the length of the access region, L_A. This length is dependent on device design and is majorly limited by fabrication challenges. One way of reducing the access resistance is by fabricating GFETs with self-aligned top-gates, where L_A is reduced to zero. There have been a few attempts of fabricating GFETs with self-aligned gates, but the fabrication processes employed are not straightforward and cannot be used in a large-scale wafer integration flow. Table 4.1 gives an outline of some examples of self-aligned GFETs from literature.

Work	**Fabrication flow**	**Notes**
D. B. Farmer *et. al.* [71]	Gate-first, followed by ALD Al_2O_3 spacer layer and source/drain deposition using gate as mask	L_A = 20 nm; 3X improvement in drive currents and g_m over un-aligned devices
L. Liao *et. al.* [72]	Self-aligned triangular nanowire gate transferred using a physical assembly process	Contact between the GaN nanowire and graphene acts as a Schottky barrier dielectric; L_G = 100 nm
A. Badmaev *et. al.* [73]	T-gate structure patterned using a dual resist process (PMMA and P(MMA-MAA))	L_A = 40 nm; L_G = 110 nm; requires angle deposition of source/drain metal

Table 4.1: A few literature reports of self-aligned GFET fabrication

In the gate-first process developed by IBM [71] the top-gate metal is deposited first over a top-gate dielectric and this is used as a mask to deposit the source/drain metals, separated by a thin ALD Al_2O_3 layer as the spacer. The most innovative step in this flow is the fact that ALD does not occur on pristine graphene. The spacer layer thus grows only on the top-gate side-walls, but not on the exposed graphene regions. This is practically not feasible, since there are always impurities on the graphene and

there would be undesired ALD deposition.

L. Liao *et. al.* [72] use highly doped GaN nanowires as the top-gate. A Schottky-like barrier is formed between the nanowire and graphene which prevents significant charge leakage. An interface depletion layer is created in the nanowire functioning as a "semi-high-k" gate dielectric. The nanowires are placed on the graphene channel using a physical assembly process which is clearly not scalable.

A. Badmaev *et. al.* [73] use a T-gate approach, where a dual-resist process using PMMA and P(MMA-MAA) is used for the top-gate metal patterning. The top-gate metal (Al) is directly deposited and when it is exposed to ambient, a thin layer of Al_2O_3 is formed at the interface. This is followed by deposition of the self-aligned source/drain metal layers using the T-gate as a mask. Since the top-gate is T-shaped, the source/drain electrodes and the top-gate do not short out.

The three fabrication methods described above are not easy to implement and might not be scalable. A simple method of reducing the series access resistance using surface-transfer doping was developed in this work and is described in the following sections.

Doping graphene shifts its Dirac voltage to higher or lower voltages depending on the type of dopant used. Pristine graphene has its Dirac voltage at 0 V where the resistance goes to its maximum value. By doping graphene, its resistance at 0 V bias can be reduced multifold. This reduction of resistance when employed to the source/drain access regions can result in an improvement of transistor performance. A fabrication process-flow was developed to dope these access regions in a self-aligned manner. With the right choice of dopants, the access regions can now be doped and the access region resistance can be modulated accordingly. Up to a $\sim$ 4X improvement in drive currents and transconductances was observed. This approach also works on insulating substrates and is easily scalable.

4.2 Fabrication process-flow

The fabrication process-flow employed to fabricate self-aligned GFETs with surface transfer doped source/drain access regions is described in this section. A schematic fabrication process-flow starting from as-fabricated GFETs is shown in Figure 4.2.

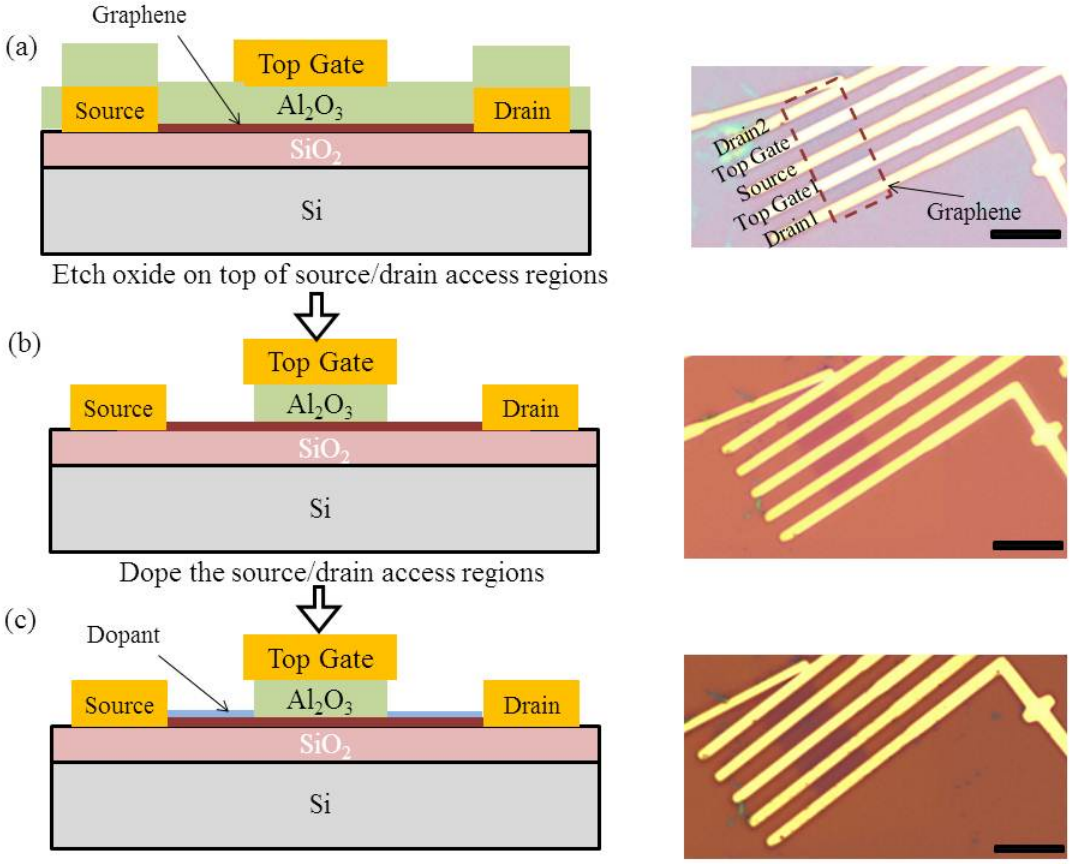
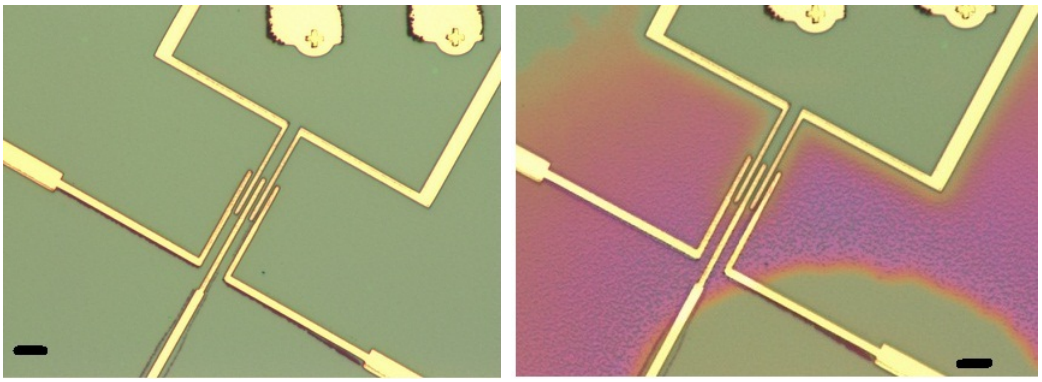


Figure 4.2: A schematic showing the fabrication process-flow employed in self-aligned GFET access region doping. Optical micrographs at the corresponding process step are shown on the right (scale bars are 10μm)

As-fabricated top-gated GFETs have ALD Al_2O_3 on top of the source/drain access regions. In order to dope the access regions, this oxide has to be etched away. A dry etch of this oxide would ideally be preferred, since it would minimize undercut below the top-gate. But, all dry-etch recipes for etching Al_2O_3 use some kind of plasma,

which is not compatible with graphene. Plasma can react with graphene, or in the worst case it can directly etch it away. Hence, a wet-etch process using dilute HF was selected. This would generate some undercut, but by using a thin top-gate dielectric, the amount of undercut can be reduced.

Buffered Oxide Etch (BOE) was used to etch the oxide on top of the source/drain access regions in the first batch of devices. This generated a large undercut, sometimes totally etching away the dielectric under the top-gate. Figure 4.3 shows optical micrographs of a device before and after etching with BOE. This etch was done to open windows on top of the source/drain metal pads to test the device before the self-aligned etch. This particular device had a pad close to the active region and Figure 4.3(b) shows the appearance of a circular etch undercut pattern around the device active region.



(a) Before BOE etch (b) After BOE etch

Figure 4.3: Appearance of undercut after etching with BOE (scale bars are 20μm)

To address this problem of excessive undercut, dilute HF (1:50) was used as an etchant for the self-aligned etch. The etch rate was calculated from experiments to be around 1 nm/s. With typical top-gate dielectric thicknesses of 20 nm, a 20 s etch was required. The sample was then cleaned in running de-ionized (DI) water for a minute and dipped in iso-propyl alcohol (IPA) for a minute to drive away adsorbed

water.

Electrical measurements made after the self-aligned etch showed a large hysteresis in the back-gate voltage sweeps. This was probably from adsorbed water molecules from the HF etch and DI water rinse steps. Details of the electrical measurements are discussed in a later section. To reduce hysteresis, the samples were pumped down to $\sim 1{\times}10^{-6}$ mbar in the Lakeshore probe station and the adsorbants were allowed to desorb for 2 days before doping the access regions.

The access regions were doped using the spin-on-doping technique discussed in Chapter 3. This allows for fine control on the amount of doping and consequently offers a control of the series access resistance.

4.3 Spin-on-doping with PEI

PEI (polyethylene imine) was chosen as the dopant for self-aligned doping of the source/drain access regions, since it is best suitable for a spin-on-doping approach. PEI also doesn't leave residues on the graphene surface and would make it possible for further processing to be done on the GFET after doping.

4.3.1 Doping process flow

Figure 4.4 shows a schematic of the spin-on-doping approach used to dope GFETs. A dilute solution of PEI in methanol (0.02% w/w) was used as the dopant. The dopant solution preparation was done using a 2-step approach. A 1% w/w solution of PEI in methanol was first prepared by weighing required quantities of PEI and methanol and stirring them together in a dark, sealed container for 2 days using a magnetic-stirrer. A small amount of this solution was then diluted to 0.02% and was again magnet-stirred for 2 days to ensure a homogeneity in the dopant solution. It

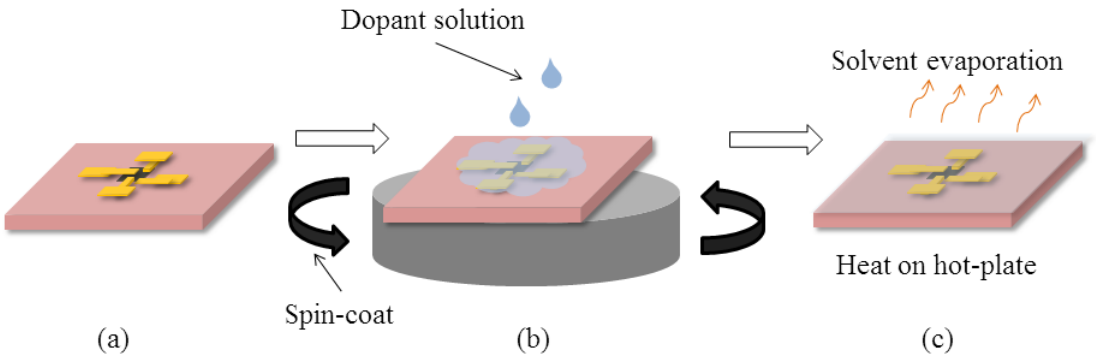


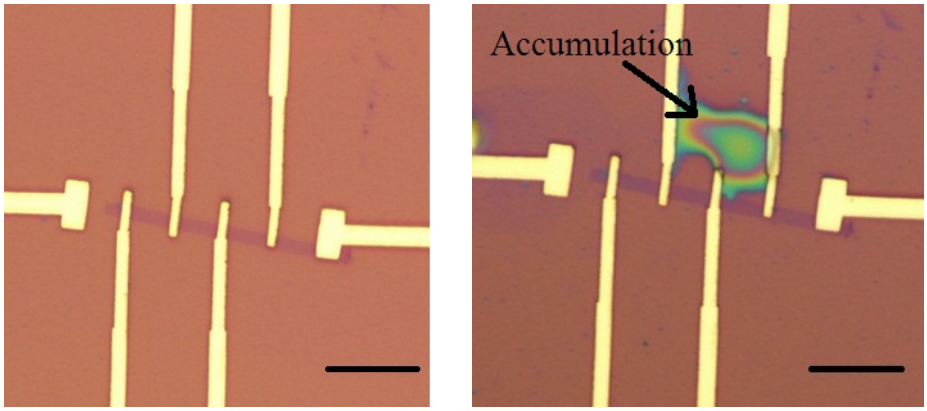
Figure 4.4: A schematic of the spin-on-doping process employed to dope GFETs

was found that this dopant solution stayed stable and homogeneous for many months when stored in sealed dropper bottles.

The dopant solution was then spin-coated onto the substrates of interest. A moderate spin-speed of 1500 rpm was chosen to ensure dopant uniformity on the substrate and at the same time ensure that the graphene does not rip due to high spin speed. Spin speeds above 2000 rpm were found to create rips and tears in the graphene. A long, 60 second spin time was chosen to ensure that there were minimal solvent residues after spin-coating.

The substrates were then heated on a hot-plate at 90°C for 20 seconds to further drive away any remaining methanol residues. PEI being a heavy macromolecule (MW 750,000) does not evaporate during this short bake step. No discernible optical color difference on the substrate was noticed after doping. However, if the substrate had any kind of impurities on it, the dopant would accumulate as a blotch around them. Figure 4.5 shows optical micrographs of a back-gated GFET on which there was accumulation of the dopant as a blotch around the graphene active region after spin-on-doping. In most cases, the impurities causing dopant accumulation were PMMA residues and this problem was mitigated by thoroughly cleaning the substrates in

acetone before doping them.



(a) Before PEI doping (b) Dopant accumulation after doping

Figure 4.5: Optical micrographs showing accumulation of PEI when the substrates are unclean (scale bars are 10μm)

In cases when there was dopant accumulation on the device active region, a large shift in Dirac voltage was observed, corresponding to a large dopant dose. Substrates with dopant accumulation were rinsed in copious amount of running methanol to wash away the dopants. The substrates were then re-cleaned in acetone to get rid of PMMA residues and other impurities and were reused for doping.

4.3.2 PEI spin-on-doped back-gated GFETs

Back-gated GFETs with 4-point probe structures were used to characterize the effect of PEI spin-on-doping on graphene. GFETs were spin-on-doped with the 0.02% PEI solution multiple times and electrical measurements taken after every doping step. Figure 4.6 shows 4-point resistivity measurements as a function of V_{BG} for a back-gated GFET after successive spin-on-doping steps. The Dirac voltage can be seen to move to a more negative voltage with every successive spin-on-doping step.

There is a reduction in the graphene 4-point resistivity at 0 V back-gate bias from 4.4 kΩ to 1.5 kΩ after doping, a 3X reduction [74]. This reduction in resistivity

when employed to the source/drain access regions of a top-gated GFET leads to improvement in GFET performance metrics.

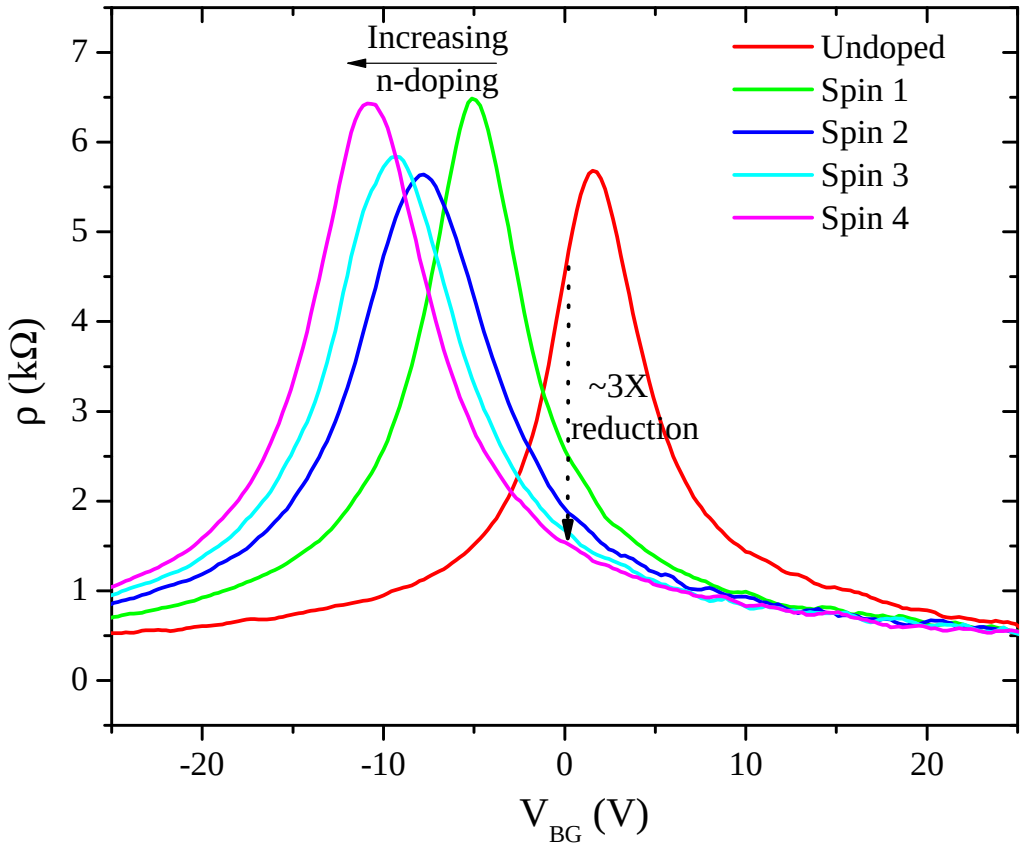


Figure 4.6: 4-point resistivity vs. V_{BG} after successive PEI spin-on-doping steps

It can also be seen from Figure 4.6 that the graphene resistivity at the Dirac voltage does not follow a particular trend, but varies randomly after each doping step (increases from the undoped case to spin 1, reduces from spin 1 to spin 2, remains more or less the same from spin 2 to spin 3 and increases after spin 4). Resistance at the Dirac voltage is related to the impurity carrier concentration and electron-hole puddles at the surface of graphene [17]. A higher impurity carrier concentration leads to a lower resistance at the Dirac voltage and vice-versa. The random trend of this resistance in Figure 4.6 is probably due to redistribution of impurities on the

graphene surface after every spin. There could also be local redistribution of the dopant molecules after every spin and different configurations of hydrogen bonding among them [75]. At this stage, this is only speculation and further analysis needs to be done to better understand the reason behind this behavior.

Figure 4.7 shows a plot of the evolution of the Dirac voltage and extracted carrier mobilities with successive doping steps. The Dirac voltage shift from one doping step to the next is proportional to the amount of extra dopants introduced at that step. Since spin-on-doping is a physical process and the dopant dose is only determined by the spin-speed, the amount of extra dopants introduced after each step is ideally expected to be the same.

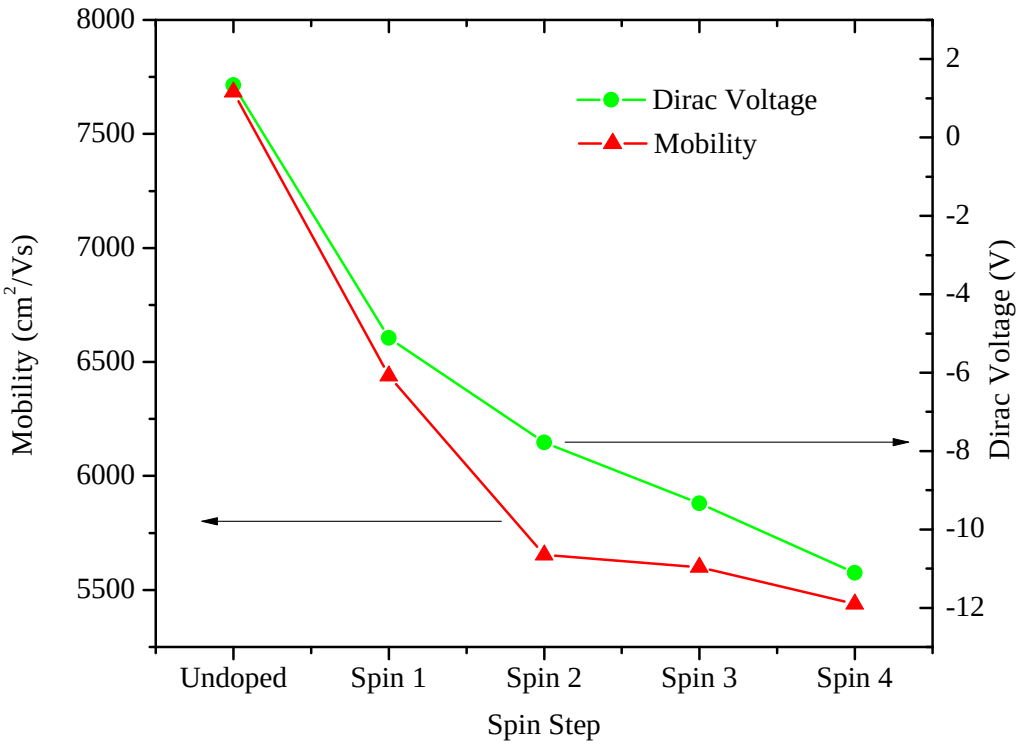


Figure 4.7: Evolution of Dirac voltage and carrier mobilities with successive doping

From Figure 4.7, it can be seen that the Dirac voltage shift produced after every spin is not the same. The same trend was observed for multiple samples and probably

has to do with the way the dopant molecules interact with each other on the graphene surface. There is also mobility degradation after every subsequent spin due to extra scattering from the dopant molecules [61].

Doping graphene n-type using PEI shifts the Dirac point to negative voltages and reduces the graphene resistance at $V_{BG} = 0$ V. This effect of doping is employed to the source/drain access regions of a top-gated GFET to achieve performance gains.

4.4 GFETs on Si/SiO_2

Top-gated GFETs were fabricated using the process flow described in Chapter 2. Electrical measurements were taken after critical processing steps and finally after self-aligned doping of the source/drain access regions. The following sections discuss the measurements and their implications.

4.4.1 As-fabricated top-gated GFETs

Back-gated GFETs are unintentionally p-doped from water vapor, PMMA residues and other impurities on the graphene surface. There could also be regions with multiple Dirac voltages on the graphene surface which show up as secondary Dirac voltages in the resistance profile.

Figure 4.8 shows the 2-point resistance between the source and drain as a function of V_{BG} for a back-gated GFET and for the same GFET after depositing the Al_2O_3 top-gate dielectric (the device dimensions are $W_G/L_G = 7.0\mu m/4.0\mu m$; 20 nm Al_2O_3). The resistance profile of the back-gated GFET (without the top-gate dielectric) shows a primary Dirac voltage at $\sim +$ 12 V and a secondary Dirac voltage at $\sim +$ 6 V. This p-type doping is unintentional. However, both these Dirac voltages move to 0 V after depositing the top-gate dielectric. This is from charge neutralization at the

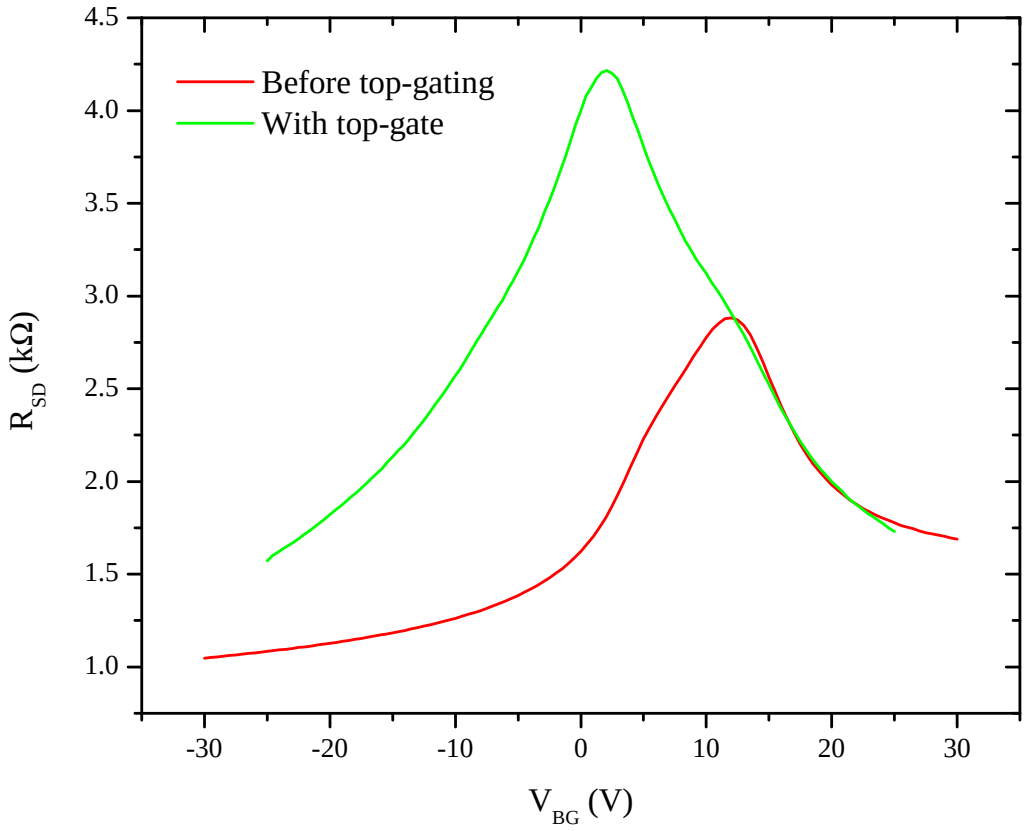


Figure 4.8: 2-point resistance vs. V_{BG} before and after top-gate deposition

graphene-Al_2O_3 interface during ALD growth [76]. The carrier mobility reduces from 6500 cm^2/Vs to 4500 cm^2/Vs after ALD deposition. This reduction in mobility, as discussed in Chapter 2 is due to charged impurities at the graphene-Al_2O_3 interface [41].

4.4.2 Post HF-etch measurements

To dope the source/drain access regions, Al_2O_3 from the source/drain access regions was etched away using dilute HF as an etchant and electrical measurements were taken after this step. Figure 4.9 shows the drain current (at V_D = 20 mV) as a function of V_{BG} at different top-gate biases for a top-gated GFET after etching away

Al_2O_3 from the source/drain access regions.

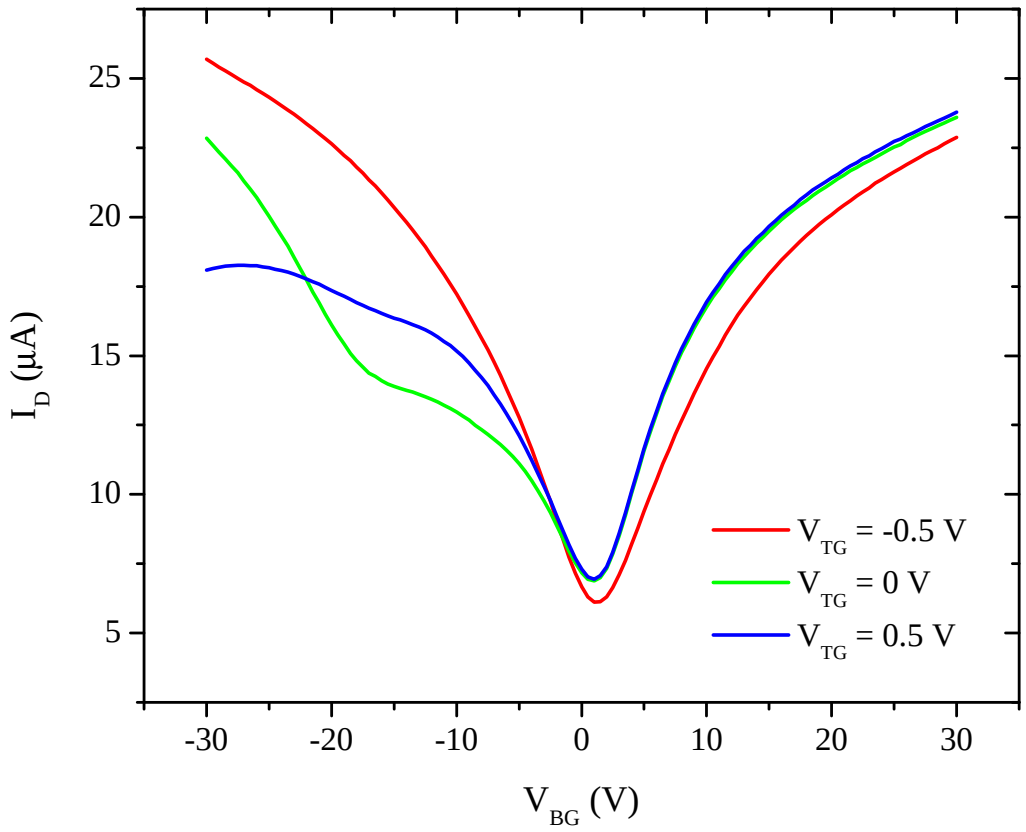
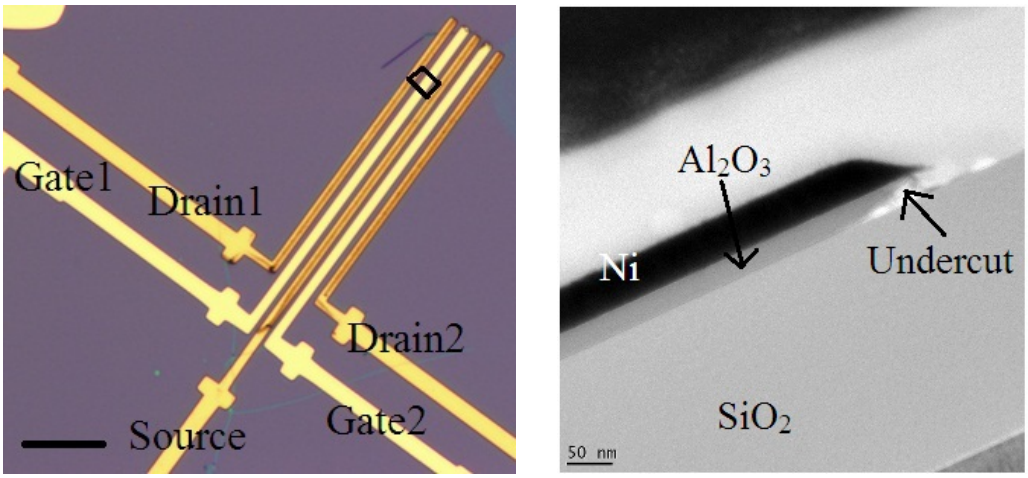


Figure 4.9: Drain current vs. V_{BG} at different top-gate biases for a top-gated GFET

An interesting effect of the self-aligned etch is that it causes the top-gated graphene's Dirac voltage to shift to a negative value, as evident from the I-V at V_{TG} = 0 V in Figure 4.9. The Dirac voltage of the top-gated region shows up as a secondary Dirac voltage at around - 17 V. The Dirac voltage of the source/drain access regions however remains at 0 V (the primary Dirac voltage). This is confirmed by back-gate voltage sweeps at non-zero top-gate bias, which selectively modulate only the top-gated graphene region. At V_{TG} = - 0.5 V, the secondary Dirac voltage disappears and the I-V has only one Dirac voltage at $\sim$ 0 V. This is because a negative V_{TG} causes the top-gated graphene to get depleted of electrons and effectively makes it undoped with respect to the back-gate, driving its Dirac voltage to 0 V.

Similarly, $V_{TG} = +0.5$ V results in the secondary Dirac voltage shifting to beyond - 30 V, which is due to accumulation of electrons in the top-gated region. This is seen as downward curving of the I-V around - 30 V when $V_{TG} = +0.5$ V in Figure 4.9. The Dirac voltage itself lies outside the back-gate sweep range and is not fully captured. A faint secondary Dirac voltage remains at - 17 V, which could be due to the graphene region at the edges of the top-gate (or graphene below the undercut region of the top-gate dielectric) which is not modulated by the top-gate.

To check the amount of undercut below the top-gate from the self-aligned etch, cross sectional TEM imaging was done on a device. Figure 4.10(a) shows the optical micrograph of the device, with the region of interest under the top-gate marked by a black box. Figure 4.10(b) is a cross-sectional TEM image showing undercut below the gate. The undercut is higher near the Al_2O_3-graphene interface, which maybe due to higher diffusion of the etchant along the interface.



(a) Optical micrograph (scale bar is 10μm) (b) Cross-sectional TEM image

Figure 4.10: Optical micrograph and TEM image after HF etch

One reason for n-doping of the top-gated graphene region after the self-aligned etch could be due to absorption of HF into the dielectric layer, which then interacts

with the graphene to dope it n-type [77]. The ungated source/drain access regions would also have HF adsorbed on them from the etch-step, but a thorough clean and vacuum treatment would get rid of them, while the HF molecules lodged in the Al_2O_3 layer would stay put, thereby doping graphene n-type under the top-gate.

4.4.3 Doped GFETs

Etching away Al_2O_3 from the source/drain access regions exposes the graphene underneath which can then be doped to reduce its resistance at $V_{BG} = 0$ V. Figure 4.11 shows back-gated 2-point resistance measurements of the device before and after spin-on-doping with 0.02% PEI (top gated region $W_G/L_G = 7.0\mu m/1.0\mu m$, $L_A = 1.5\mu m$).

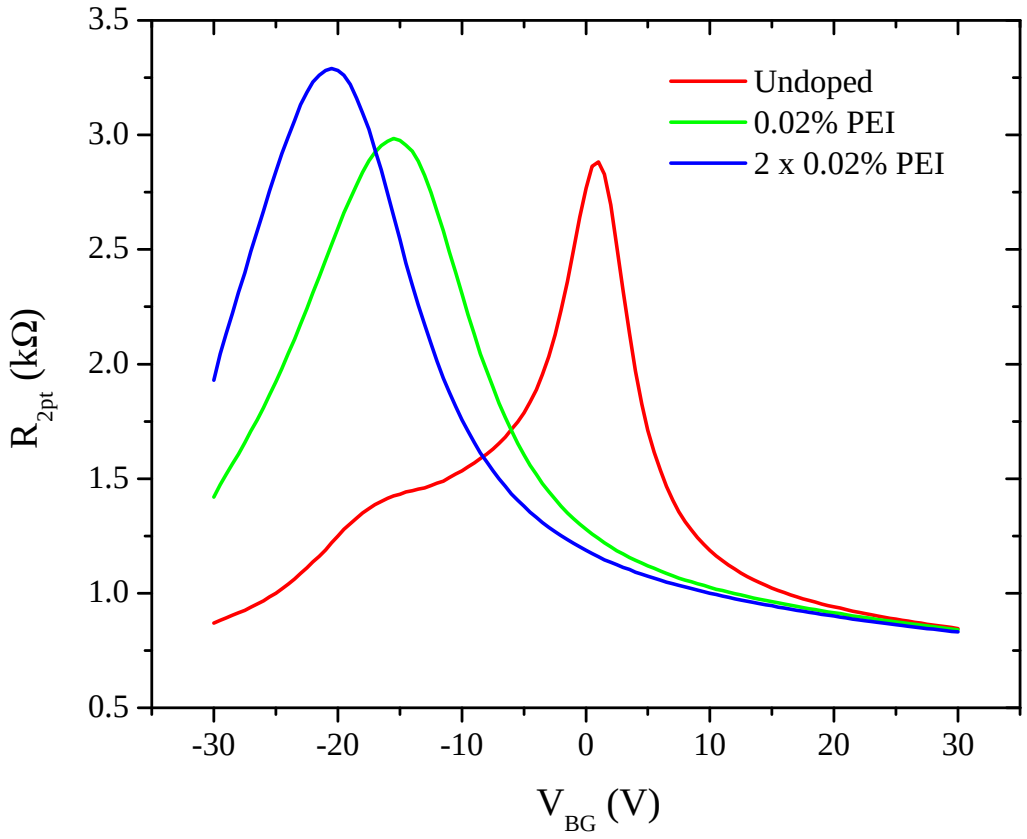


Figure 4.11: 2-point resistance vs. V_{BG} (at $V_{TG} = 0$ V) before and after doping the source/drain access regions

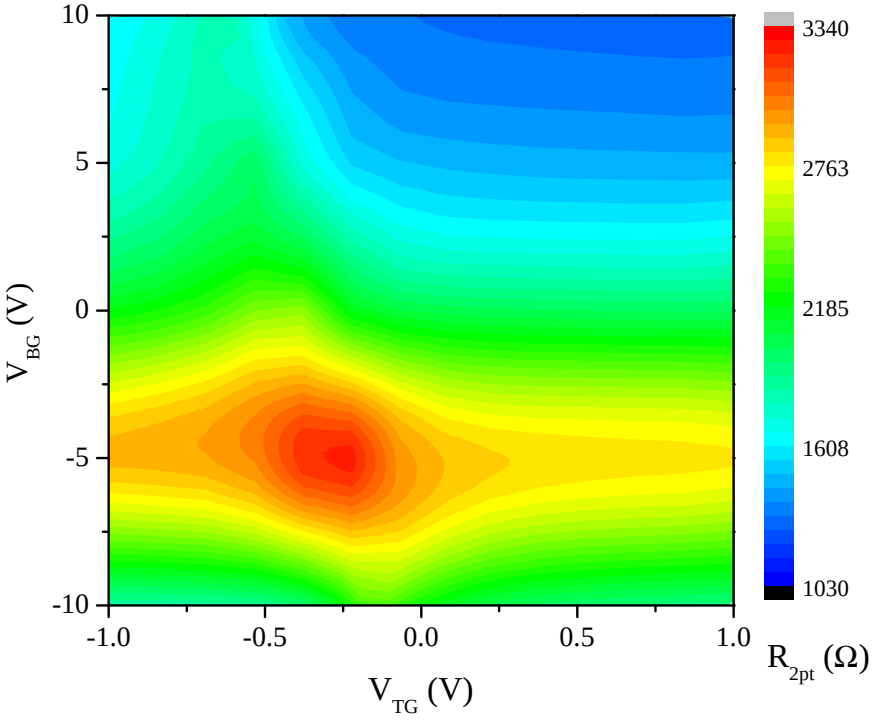
The undoped resistance profile has a familiar shape corresponding to two Dirac voltages: the primary Dirac voltage at 0 V from the source/drain access regions and a secondary Dirac voltage at - 17 V from the top-gated graphene. Only the source/drain access regions get doped and the primary Dirac voltage moves to a negative value, while the top-gated graphene's Dirac voltage remains unchanged at - 17 V.

There is a broadening of the resistance curve after doping which is due to the presence of two regions of graphene with slightly mismatched Dirac voltages (the top-gated region at - 17 V and the access regions at $\sim$ - 13 V). This makes it difficult to extract carrier mobilities for such a structure with different regions of different Dirac voltages.

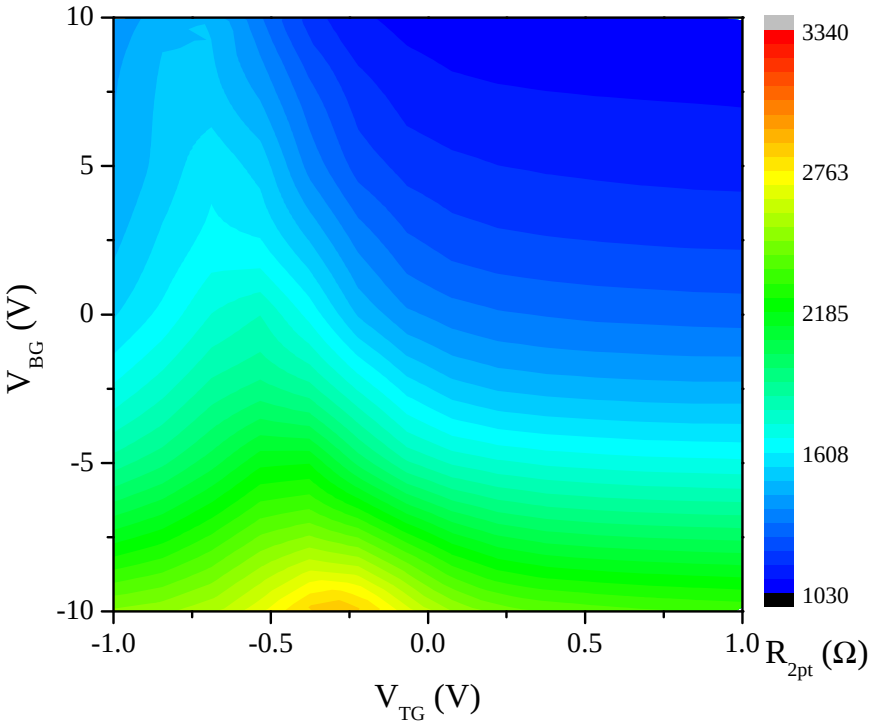
Figure 4.11 also shows the 2-point resistance after a second spin-coating step, which moves the Dirac voltage of the ungated regions to an even more negative value. The parameter of interest in these resistance profiles is the resistance at $V_{BG} = 0$ V, which reduces from 2.8 kΩ in the undoped case to 1.2 kΩ after doping and 1.1 kΩ after doping the second time.

The reduction in resistance is only from the source/drain access regions. This is better understood by looking at Figure 4.12 which shows 2-point resistance measurements as a function of both the back-gate and top-gate biases before and after doping the source/drain access regions. The Dirac voltage of the top-gated region is not effected by doping. This is apparent from the position of the resistance peak at - 0.3 V (when referred to the top-gate) before doping (Figure 4.12(a)), which still remains at - 0.3 V after doping (Figure 4.12(b)). Doping the source/drain access regions only induces a shift of the resistance profile to a negative V_{BG}, keeping the profile along V_{TG} invariant.

Figure 4.13 shows transfer characteristics of the device before and after doping. The maximum drive current ($I_{D,max}$) increases from 7.6 μA to 16.6 μA (a factor of



(a) Before Doping



(b) After Doping

Figure 4.12: 2-point resistance profiles as a function of V_{BG} and V_{TG}

2.2X) and the transconductance (g_m) from 4.2 μS to 10.3 μS (a factor of 2.5X) after doping [74]. There is also an improvement in I_{ON}/I_{OFF} by 20% after doping.

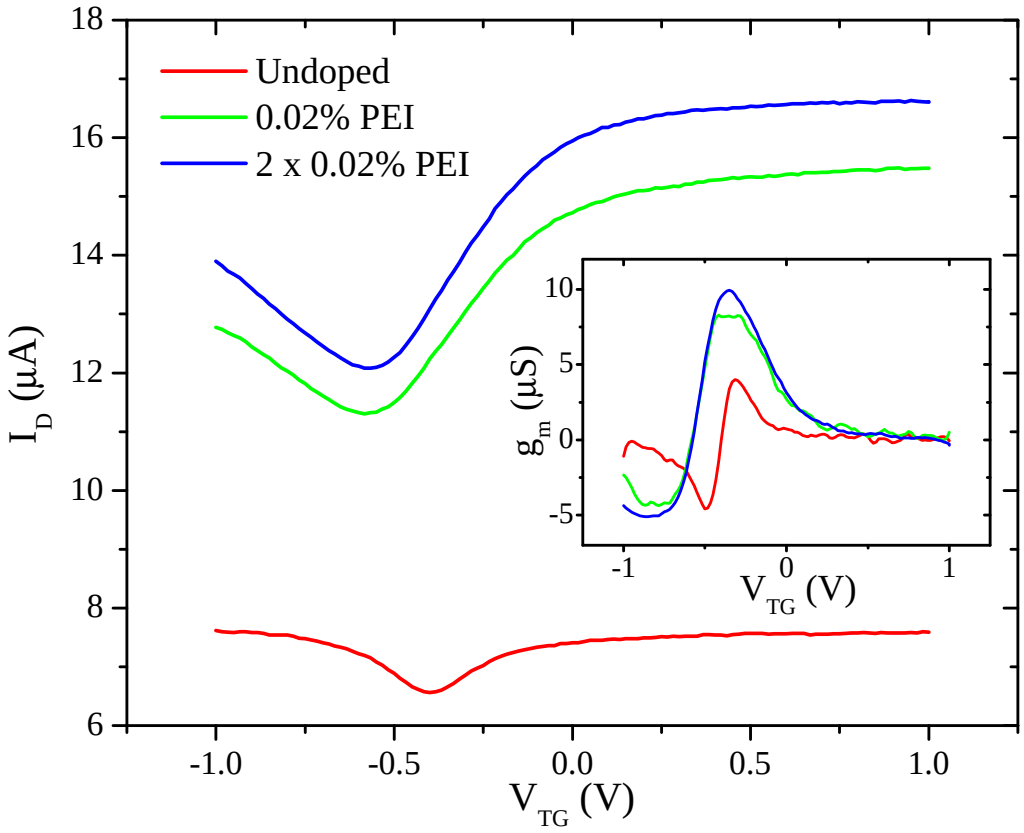


Figure 4.13: I_D-V_{TG} and g_m-V_{TG} (inset) of the device before and after doping

This improvement in device characteristics is dependent on the device layout, specifically the length of the source/drain access regions (L_A) with respect to the top-gated graphene region (L_G). For a typical top-gated GFET with $L_A = L_G$ (in this case, $L_A = 1.5 \times L_G$), there is a drive current improvement of around 2X. In devices with longer L_A (say, $L_A = 3 \times L_G$), it is possible to get up to a 4X improvement (results for this device are not presented here).

4.5 GFETs on quartz

Top-gated GFETs on single crystal, atomically smooth quartz substrates are better suited for radio frequency (RF) applications than GFETs on Si/SiO_2. The insulating nature of quartz leads to lower parasitic capacitances and results in higher GFET operating frequencies. Quartz substrates are ideal for low loss and temperature stable high-frequency electronics [30]. The absence of a back-gate on quartz makes it impossible to electrostatically modulate the source/drain access resistance. Self-aligned doping can be used effectively in this case to reduce the access resistances.

4.5.1 Fabrication of GFETs on quartz

Graphene cannot be exfoliated on quartz substrates because of the lack of optical contrast. In order to fabricate top-gated GFETs on quartz, graphene was exfoliated on Si/SiO_2 substrates and then transferred to quartz using the transfer process shown in Figure 4.14.

Monolayer graphene was exfoliated on Si substrates with 285 nm SiO_2, identified using optical contrast and confirmed using Raman spectroscopy. The substrate was then spin-coated with a layer of 4% PMMA, followed by multiple spin-coating steps with 8% PMMA, until the PMMA layer was around 3-5 μm thick.

The substrate was then treated in a hot sodium hydroxide (NaOH) solution for 10 minutes to etch away SiO_2 and release the PMMA film (which captures the graphene). This PMMA film was rinsed in DI water and transferred to a clean quartz substrate using a wet-transfer process [78]. The PMMA film was floated on a drop of DI water on the quartz substrate and the water was let to dry out naturally. The PMMA film sticks to the quartz substrate after the water dries out. The sample was left in a vacuum desiccator for 24 hours to further remove water from below the PMMA layer.

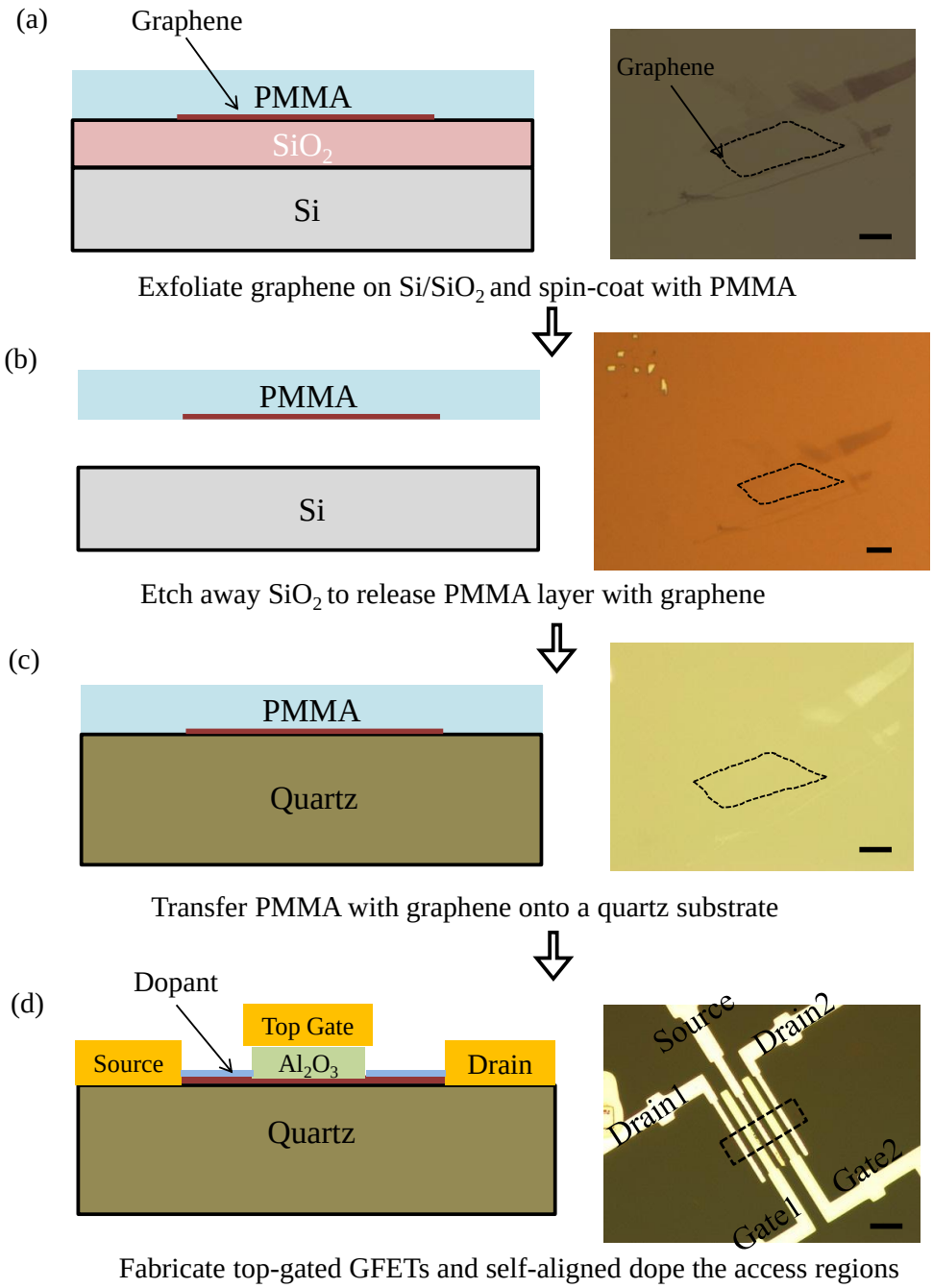


Figure 4.14: A schematic showing fabrication of top-gated GFETs on quartz substrates. Optical micrographs at the corresponding process step are shown on the right (all scale bars are 5μm)

This thick PMMA film was then etched down to around 500 nm and subsequently spin-coated with a fresh layer of 4% PMMA for further processing. The process flow after this step is almost identical to fabrication of top-gated GFETs on Si/SiO_2.

Since quartz is an insulating substrate, performing EBL on quartz leads to charging effects. These problems were avoided by spin-coating the substrates with a water-soluble conducting polymer (Espacer 300Z) before EBL [79].

4.5.2 Electrical measurements

The insulating nature of quartz makes it impossible to take back-gated I-V measurements of GFETs on quartz. Electrical measurements are possible only after depositing the top-gate stack. Figure 4.15 shows the transfer characteristics of a top-gated GFET on quartz before and after doping the source/drain access regions with a 0.02% PEI dopant solution.

There is an improvement in maximum drive current ($I_{D,max}$) by a factor of $\sim$ 2X and an improvement in transconductance (g_m) by a factor of $\sim$ 3X after doping. The on/off current ratio (I_{ON}/I_{OFF}) also increases by 10% after doping. There is very little degradation in carrier mobility from 5600 cm^2/Vs to 5200 cm^2/Vs after doping. The device dimensions are W_G/L_G = 7.0 μm/2.0 μm; L_A = 1.8 μm.

The top-gated graphene region has its Dirac point close to 0 V before the self-aligned doping. This is in contrast to the GFET on Si/SiO_2 which had its Dirac point at a negative voltage before doping. This difference in behavior was consistently observed in various samples and the reason is not known.

Figure 4.16 shows the transfer characteristics of the GFET before and after doping. There is an improvement in the drain currents by a factor of $\sim$ 2X.

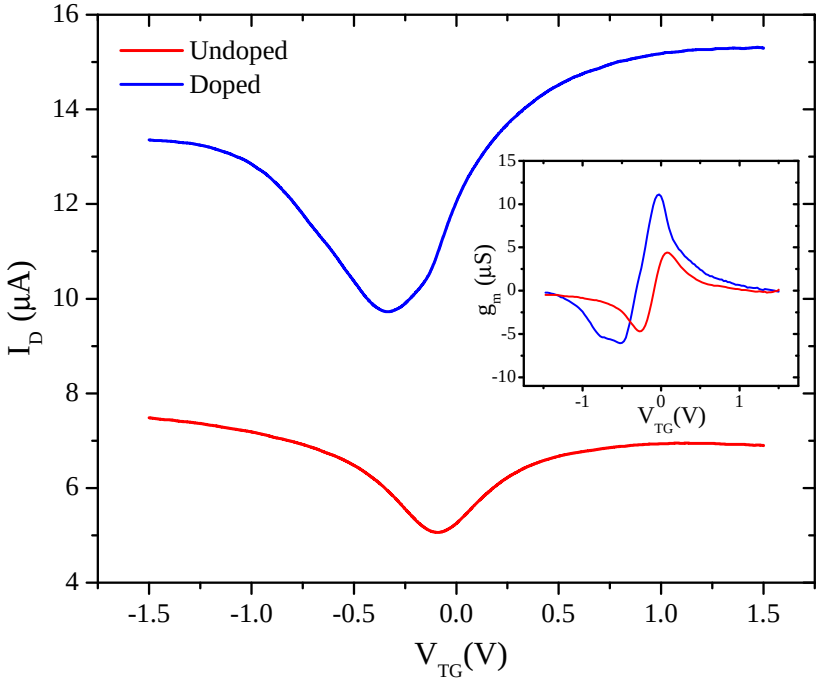


Figure 4.15: I_D-V_{TG} and g_m-V_{TG} (inset) of a GFET on quartz before and after doping

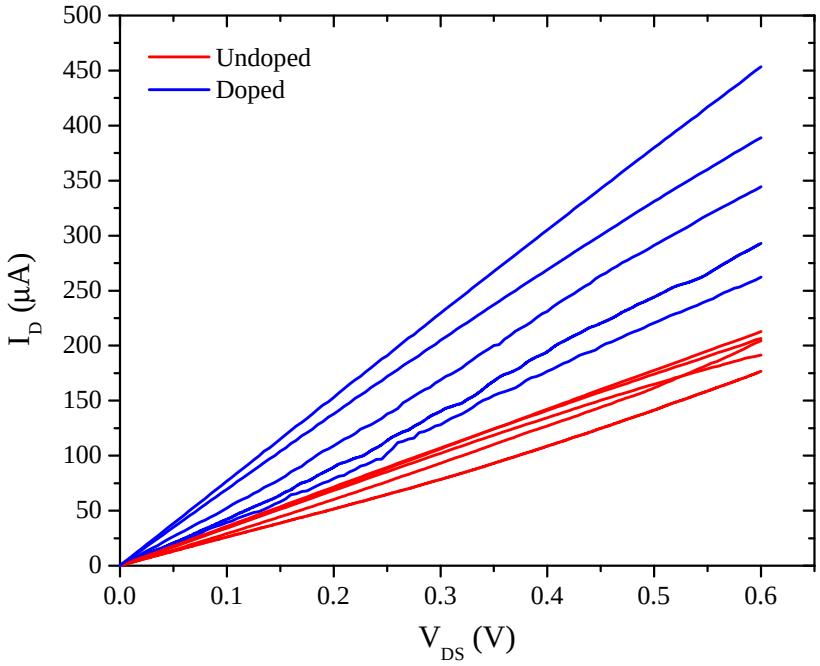


Figure 4.16: I_D-V_{DS} before and after doping (V_{TG} - V_{DIRAC} is swept from 0 V to 1 V in steps of 0.25 V)

4.6 Summary

The series resistance contribution from the source/drain access regions of top-gated GFETs is a major factor responsible for degradation of their performance. GFETs with self-aligned gates overcome this problem, but their fabrication is not straightforward.

A simple way of reducing the source/drain access resistance is by doping them with surface transfer dopants which shift the Dirac voltage to a negative value and effectively reduces the graphene resistance at 0 V back-gate bias. A fabrication process-flow for doping these access regions using the top-gate as a self-aligned mask was developed. A novel method of spin-on-doping with a 0.02% PEI solution in methanol was used to dope graphene. Spin-on-doping offers a control of the amount of doping through repetitive spin-coating steps.

Top-gated GFETs were fabricated on Si/SiO_2 substrates and prepared for self-aligned doping by etching away oxide on top of the access regions. The GFETs showed a 2X improvement in maximum drive currents ($I_{D,max}$) and transconductances (g_m) after doping, with a maximum 4X improvement depending on the device layout.

To fully utilize the advantage of self-aligned doping, top-gated GFETs were fabricated on quartz substrates, where the absence of a back-gate makes it impossible to modulate the access resistances electrostatically. Mobilities up to 5,600 cm^2/Vs were observed with enhancement in GFET performance by around 2X after doping.

5

Conclusions

5.1 Thesis summary

With CMOS scaling giving only marginal improvements in device performance over time, novel materials are being explored to replace silicon in integrated circuits. The high carrier mobilities and saturation velocities of graphene coupled with its ease of synthesis make it a promising alternative for silicon.

Methods of identifying and characterizing graphene using optical microscopy, Raman spectroscopy and AFM have been presented. Process flows for fabricating back-gated and top-gated GFETs with high-κ top-gate dielectrics were developed using standard cleanroom processes. A model was presented to extract carrier mobilities and residual carrier concentrations from the electrical measurements of GFETs. Back-gated GFETs using exfoliated monolayer graphene showed carrier mobilities up to 9,400 cm^2/Vs and CVD graphene GFETs showed carrier mobilities up to 1,300 cm^2/Vs at room temperature. The effects of unintentional doping and hysteresis on GFETs were investigated. Top-gated GFETs with ALD Al_2O_3 top-gate dielectrics showed carrier mobilities up to 8,500 cm^2/Vs.

A literature survey of doping graphene using substitutional methods and surface transfer methods and methods of characterizing doped graphene were presented. The effects of surface transfer doping using PMMA, TCNQ and PEI on the electronic properties of graphene were investigated in detail. PEI was chosen as the preferred dopant due to its ease of doping and its negligible effect on the carrier mobilities of graphene. Doping loss from graphene and methods to prevent doping loss using ALD capping layers were discussed.

Finally, surface transfer doping with PEI was used to chemically dope the source and drain access regions of top-gated GFETs in a self-aligned manner to reduce their access resistances and improve device characteristics. A novel method of spin-on-doping PEI onto graphene was developed for this purpose. Up to a 4X improvement in drive current ($I_{D,max}$) and transconductance (g_m) was observed after doping. Top-gated GFETs were also fabricated on quartz substrates and self-aligned doped to result in up to a 2X improvement in device performance, with carrier mobilities of 5,600 cm^2/Vs.

5.2 Future work

Surface transfer doping using metal adatoms and gases: This thesis investigated surface transfer doping of graphene using organic polymer materials. Evaporated metal adatoms like Bi, Sb and Au and adsorbed gases like NH_3, NO_2 and SO_2 also have the potential to dope graphene. Application of these dopants on graphene could be more challenging but could offer better control of the amount of doping and could even open a bandgap in graphene [18].

Doped bilayer graphene and bilayer GFETs: Doping can be an easy way of opening a bandgap in bilayer graphene. It is known that a bandgap can be

opened in bilayer graphene by the application of a large electric field perpendicular to the graphene plane. Selectively doping bilayer graphene from the top or bottom can give an additional knob to control the bandgap and also its electronic properties [14].

Self-aligned doped radio frequency (RF) GFETs: GFETs on insulating substrates like quartz are better suited for RF applications due to the lower parasitic capacitances offered by these substrates [30]. Self-aligned chemical doping of the source/drain access regions of these GFETs could be an easy way of improving their RF performance. The mobility asymmetry induced by PEI could also be put to a constructive use in these devices.

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